Bitline/Plateline Reference-Level-Precharge Scheme For High-Density Chain FeRAM

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This paper proposes a new bitline/plateline precharge and driving scheme for high-density 32Mb chain FeRAM. Both bitline and plateline are precharged to reference level, and cell data is readout by applying bias to ferroelectric capacitor by pulling up plateline and pulling down bitline in access. This scheme suppresses both reliability degradation of cell transistors and signal-loss inherent to chain FeRAM architecture. Furthermore, this reference level precharge scheme reduces the active power dissipation by 10%.