A High-Speed 128Kbit MRAM Core for Future Universal Memory Applications

A. Bette[1], J. DeBrosse[2], D. Gogl[1], H. Hoenigschmid[1], R. Robertazzi[3];
C. Arndt[1], D. Braun[1], D. Casarotto[1], R. Havreluk[3], S. Lammers[1],W. Obermaier[1],W. Reohr[3], H.Viehmann[1];
W. J. Gallagher[3] and G. Müller[1].

[1] Infineon Technologies, [2] IBM Microelectronics Division, [3] IBM Watson Research Center,
MRAM Development Alliance, IBM/Infineon Technologies, IBM Semiconductor Research and Development Center,
2070 State Route 52, Hopewell Junction, NY 12533, USA

A 128Kb MRAM (Magnetic Random Access Memory) test chip has been fabricated utilizing for the first time a 0.18µm, VDD = 1.8V, logic process technology with Cu backend of line. The presented design uses a 1.4µm^2 1T1MTJ (1-Transistor/1-Magnetic Tunnel Junction) cell and features a symmetrical high-speed sensing architecture using complementary reference cells and configurable load devices. Extrapolations from test chip measurements and circuit assessments predict a 5ns random array read access time and random write operations with <5ns write pulse width.