Destructive-read Random Access Memory System Buffered with Destructive-read Memory Cache for SoC Applications

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Abstract

A novel random access memory system, based on a destructive read memory buffered by a destructive read memory cache for hidden write back, is demonstrated. Limited only by the destructive read time, the system can achieve SRAM comparable random access cycle time (tRC). By using a DRAM array as cache, the silicon area is reduced by about 25% from the SRAM cache system. Write back algorithms have been proved by mathematical models, and confirmed by simulations.