A 0.18μm Logic-based MRAM Technology for High Performance Nonvolatile Memory Applications

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2Kb to 128Kb MRAM test chips with cell sizes of 1.4 – 1.7μm^2 were fabricated in a 0.18μm, 3 level Cu logic based process. Outlined here is a yield analysis of the read operation, which is governed by the MTJ resistance distribution function and a systematic study of the write operation. MRAM functionality, with a checkerboard disturb pattern, was obtained after process optimization. Write endurance tests did not show degradation of the cell properties.