Design Guideline of HfSiON Gate Dielectrics for 65 nm CMOS Generation

T. Watanabe, M. Takayanagi, R. Iijima[**], K. Ishimaru, H. Ishiuchi and Y. Tsunashima[*]

SoC Research & Development Center, [*]Process & Manufacturing Engineering Center, Toshiba Corporation Semiconductor Company,

[**] Advanced LSI Technology Laboratory, Corporate Research & Development Center, Toshiba Corporation,

8 Shinsugita-cho, Isogo-ku, Yokohama, Kanagawa 235-8522 Japan

Phone: +81-45-770-3644 Fax: +81-45-770-3571 E-mail: ta.watanabe@toshiba.co.jp

We investigated the characteristics of sub-100nm CMOSFETs with various C_{Hf} and provided a design guideline of HfSiON from the viewpoint of device performance. It was pointed out that C_{Hf} is responsible for parasitic resistance of short channel MOSFET. C_{Hf} should be kept low if it meets the I_g target to obtain superior MOSFET performance. Moreover, CMOSFETs with optimized HfSiON was demonstrated, providing a potential solution for 65 nm CMOS generation.