High Performance 35 nm Gate CMOSFETs with Vertical Scaling and Total Stress Control for 65 nm Technology

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Abstract

High performance 35 nm gate CMOSFETs for 65 nm technology node is demonstrated. The impact of vertical gate scaling on poly-Si gate dopant activation annealing and device performance is investigated. Total stress controls improved the nMOS drive-current up to 5-10%. Excellent controlled 35 nm gate CMOSFETs are achieved with a high drive current of 650uA/um for nMOS and 310uA/um for pMOS at Ioff=70nA/um at Vd of 0.85V. Low CV/I values of 0.85ps for nMOS and 1.61ps for pMOS are obtained.