Technologies for Scaling Vertical Transistor DRAM Cells to 70nm

R. Divakaruni, C. Radens, M. Belyansky, M.Chudzik, D.-G. Park, S. Saroop, D. Chidambarrao, M.Weybright, H. Akatsu,
L. Economikos, K. Settlemyer, J. Strane, D.Dobuzinsky, N. Edleman, G. Feng, Y.Li,, R.Jammy, E.Crabbé, and G.Bronner

IBM Microelectronics, Semiconductor R&D Center, Z/33A, 2070 Route 52, Hopewell Junction NY, 12533

Vertical transistor DRAM cells have been demonstrated as viable in the 110nm generation. This paper describes the issues associated with scaling these cells to the 70nm node and demonstrates fixes to all known issues. Scaling to 70nm is possible through the development of two key enabling technologies, high aspect ratio STI fill and low resistance metal deep trench fill, and through minor cell modification. Each of these items are addressed and shown to be viable using a functional 512Mb prototype DRAM chip at 110nm half-pitch groundrule. Based on these results, we believe the vertical transistor DRAM cell is one of the most promising for continued scaling of conventional DRAM and embedded DRAM cells.