# A High Performance 90 nm Logic Technology with a 37nm Gate Length, Dual Plasma Nitrided Gate Dielectric and Differential Offset Spacer

B. Hornung, R. Khamankar, H. Niimi, M. Goodwin, L. Robertson, D. Miles,
B. Kirkpatrick, H. AlShareef, A. Varghese, M. Bevan, P. Nicollian ,
P.R. Chidambaram, S. Chakravarthi, A. Gurba, X. Zhang, J. Blatchford, B. Smith,
J.P. Lu, J. Deloach, B. Rathsack, C. Bowen, G. Thakar, C. Machala and T. Grider

Texas Instruments, MS 3736, 13560 N. Central Expressway, Dallas, USA.
Tel: 972-995-1564. e-mail: b-hornung@ti.com

***Abstract –*** A 90nm logic technology is presented featuring an aggressively scaled 37nm gate length, 1.3 nm EOT plasma nitrided gate dielectric with differential offset spacer and leading edge CV/I performance. NMOS and PMOS transistors have been optimized with different extension offsets for NMDD and PMDD implants, which enables independent optimization of short channel effects, parasitic capacitance and drive current. The gate dielectric meets reliability requirements at 1.2V operation. The technology includes a standard Vt (SVt) transistor, low Vt (LVt) transistor and 1.5V IO transistor with 100nm gate length and dual plasma nitrided gate dielectric.