Integration of Cu/low-k Dual-Damascene Interconnects with a Porous PAE/SiOC Hybrid Structure for 65nm-node High Performance eDRAM

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A porous PAE/SiOC(k2.5)/SiC(k3.5) hybrid Dual Damascene (DD) interconnect has been successfully integrated for 65nm-node high performance eDRAM. Excellent interconnect performance was achieved by applying Triple Hard Mask (THM) process that we have demonstrated for the first time. The porosity of porous PAE was optimized to enhance the mechanical strength to prevent process-induced damages. We found that this DD structure employing the THM process is the most promising to satisfy all the requirements for 65nm-node eDRAM.