Title:

Accurate Modeling Method for Deep Sub-Micron Cu Interconnect

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Abstract:

This paper newly proposes an accurate modeling method of the copper interconnect cross-section in which the width and thickness dependence on layout patterns and density are fully incorporated and universally expressed. In addition, we have developed specific test patterns for the model parameters extraction, and an efficient extraction flow. We have extracted the model parameters for 0.15μm CMOS using this method and confirmed that 10% τpd error normally observed with conventional LPE (Layout Parameters Extraction) was completely dissolved. This is the first time that the practical and accurate modeling methodology for layout pattern sensitive Cu Interconnect is ever reported.