SESSION – 12
Advanced FUSI Gates Stacks

Wednesday, June 14, 1:30 p.m.
Chairpersons: T. Skotnicki, STMicroelectronics
K. Shibahara, Hiroshima University

12.1 – 1:30 p.m.
Novel FUSI Strained Engineering for 45-nm Node CMOS Performance Enhancement, C.T. Lin, C.H. Hsu, L.W. Chen, T.F. Chen, C.R. Hsu, C.H. Lin, S. Chiang, D.C. Cho, C.T. Tsai, G.H. Ma, United Microelectronics Corporation, Hsin-Chu City, Taiwan

FUSI metal gate with strained engineering is extensively investigated and reported for the first time. Enveloped FUSI (Fully silicided) phase transfer and volume change induced stress exhibits 10% NMOS ION enhancement. Further, the second CESL (Contact Etch Stop Layer) induced stress raised another 8% NMOS ION gain. Although the first CESL on poly-gate top removed by FUSI CMP leads to 10% PMOS ION degradation, it can be recovered or further improved by a dual CESL process.

12.2 – 1:55 p.m.
Dual Work Function Phase Controlled Ni-FUSI CMOS (NiSi NMOS, Ni_2Si or $Ni_{31}Si_{12}$ PMOS): Manufacturability, Reliability & Process Window Improvement by Sacrificial SiGe Cap, A. Veloso, T. Hoffman, A. Lauwers, S. Brus, J.-F. de Marneffe, S. Locorotondo, C. Vrancken, T. Kauerauf, A. Shickova, B. Sijmus, H. Tigelaar, M.A. Pawlak, H.Y. Yu, C. Demeurisse, S. Kubicek, C. Kerner, T. Chiarella, O. Richard, H. Bender, M. Niwa, P. Absil, M. Jurczak, S. Biesemans, J.A. Kittl, IMEC, Leuven, Belgium

We present the first evaluation of manufacturability and reliability of dual WF phase-controlled Ni-FUSI/HfSiON CMOS. RTP1 and poly/spacer height are the most critical process control parameters. A novel sacrificial SiGe cap process opens the RTP1 process window from ~5C to ~20C for Lg down to 45nm, making CMOS Ni-FUSI manufacturable. Vt control with stdev~19 and 21mV (NMOS, PMOS) is obtained. TDDB and NBTI of NiSi, Ni_2Si and $Ni_{31}Si_{12}$ showed ~1V VDD for 10 years lifetime.

12.3 – 2:20 p.m.
Suppression Effects of Threshold Voltage Variation with Ni FUSI Gate Electrode for 45nm Node and Beyond LSTP and SRAM Devices, Y. Okayama, T. Saito, K. Nakajima, S. Taniguchi, T. Ono, K. Nakayama, R. Watanabe, A. Oishi, A. Eiho, T. Komoda, T. Kimura, M. Hamaguchi, Y. Takegawa, T. Aoyama, T. Iinuma, K. Fukasaku*, R. Morimoto*, K. Oshima*, K. Oono*, M. Saito*, M. Iwai, S. Yamada, N. Nagashima*, F. Matsuoka, Toshiba Corporation, Yokohama, Japan, *Sony Corporation, Yokohama, Japan

We have found that fully silicided (FUSI) gate is a promising technology for the first time not only for breaking the gate stack scaling limitation on low standby power devices but for keeping continuous scaling of high density SRAM (HDSRAM) for 45nm node and beyond. It is shown that FUSI will drastically suppress the fluctuation of threshold voltage of fine transistors of HDSRAM. We have confirmed that FUSI gate drastically decreses the Vth variation.

12.4 – 2:45 p.m.
Demonstration of a New Approach Towards 0.25V Low-Vt CMOS Using Ni-based FUSI, H.Y. Yu, J.A. Kittl, A. Lauwers, R. Singanamalla, C. Demeurisse, S. Kubicek, E. Augendre, A. Veloso, S. Brus, C. Vrancken, T. Hoffman, S. Mertens, B. Onsia, R. Verbeeck, M. Demand, A. Rothchild, B. Froment, M. van Dal, K. De Meyer, M.F. Li*, J.D. Chen*, M. Jurczak, P.P. Absil, S. Biesemans, IMEC, Leuven Belgium, *National University of Singapore, Singapore

This report discusses a new and practical approach to implement low Vt bulk CMOS using Ni-based FUSI MOSFETs. On the nFET, we demonstrate for the first time that incorporating Yb by ion implantation can achieve similar reduction of effective work function (WF) compared to alloying making it a candidate for CMOS integration. We complement our previous work on WF modulation by Yb on NiSi/SiON with new data on NiSi/HfSiON and NiGeSi/HfSiON. On the pFET, we study the effect of Al and Pt on Ni-rich FUSI and integrate it with a SiGe-channel. Integration into our reference devices resulted in a Vt reduction from 0.55/0.61V down to 0.30/0.25V for nFET (NiSi:Yb gate) and pFET (Ni_2Si:Pt gate + SiGe channel) respectively on SiON without degradation of the dielectric integrity and long channel mobility, and without an increase in gate leakage and Dit.