SESSION 16 – TAPA I
Strain Enhanced CMOS II

Thursday, June 15, 8:30 a.m.
Chairpersons: F. Nouri, Applied Materials Inc.
H. Matsuhashi, OKI Electric Industry Co., Ltd.

16.1 – 8:30 a.m.
Strain Controlled CMOSFET with Phase Controlled Full-Silicide (PC-FUSI)/HfSiON Gate Stack Structure for 45nm-node LSTP Devices, M. Saitoh, T. Ogura, K. Takahashi, T. Hase, A. Toda, N. Ikarashi, M. Oshida, T. Tatsumi, H. Watanabe, NEC Corporation, Kanagawa, Japan

Using Ni-FUSI/HfSiON gate with NiSi for NFET and Ni3Si for PFET, excellent CMOSFET properties (Tinv:1.8nm, Ig:7E-3 A/cm^2, Vth:+/-0.4V, Ion:510/270 uA/um, Ioff:100 pA/um) are achieved at Lg:45nm. We show Ni3Si electrode from thin poly-Si introduces compressive strain in channel, which increases hole mobility, and connecting point between NiSi of NFET and Ni3Si of PFET has abrupt interface, which suggest phase controlled full-silicidation process is suitable for the further scaling down of CMOSFET for LSTP.

16.2 – 8:55 a.m.
Strain-Enhanced CMOS Through Novel Process-Substrate Stress Hybridization of Super-Critically Thick Strained Silicon Directly on Insulator (SC-SSOI), A.V-Y. Thean, D. Zhang, V. Vartanian, V. Adams, J. Conner, M. Canonico, H. Desjardin, P. Grudowski, B. Gu, Z.-H. Shi, S. Murphy, G. Spencer, S. Filipiak, D. Goedeke, X.-D. Wang, B. Goolsby, V. Dhandapani, L. Prabhu, S. Backer, L.-B. La, D. Burnett, T. White, B.-Y. Nguyen, B.E. White, S. Venkatesan, J. Mogab, I. Cayrefourcq*, C. Mazure*, Freescale Semiconductor Inc., Austin, TX, *SOITEC, Crolles Cedex, France

This paper describes a biaxial-uniaxial hybridized strained CMOS technology achieved through selective uniaxial relaxation of thick SSOI, dual-stress nitride capping layer, and embedded SiGe source/drain. Through novel strain engineering, nFET/pFET Idsat enhancements as high as 27%/36% have been achieved for sub-40nm devices at 1V with 30% reduction in gate leakage current, while introducing minimum process complexity. This work demonstrates the scalability of SC-SSOI and its advantages over pure biaxial and single uniaxial strained Si technologies.

16.3 – 9:20 a.m.
Silicon-on-Insulator MOSFETs with Hybrid Crystal Orientations, M. Yang, K. Chan, A. Kumar, S.-H. Lo, J. Sleight, L. Chang, R. Rao, S. Bedell, A. Ray, J. Ott, J. Patel, C. D'Emic, J. Rubino, Y. Zhang, L. Shi, S. Steen, E. Sikorski, J. Newbury, R. Meyer, B. To, P. Kozlowski, W. Graham, S. Maurer, S. Medd, D. Canaperi, L. Deligianni, J. Tornello, G. Gibson, T. Dalton, M. Ieong, G. Shahidi, IBM Semiconductor Research and Development Center, Yorktown Heights, NY

Novel silicon-on-insulator (SOI) structures are presented on hybrid orientation substrates (SuperHOT), i.e. with nFETs on (100) surface orientation and pFETs on (110) orientation, using silicon lateral overgrowth. Functional SOI MOSFETs and ring oscillators are demonstrated.

16.4 – 9:45 a.m.
25nm Short and Narrow Strained FDSOI with TiN/HfO_2 Gate Stack, F. Andrieu, C. Dupre, F. Rochette, O. Faynot, L. Tosti, C. Buj, E. Rouchouze*, M. Casse, B. Ghyselen**, I. Cayrefourcq**, L. Brevard, F. Allain, J.C. Barbe, J. Cluzel, A. Vandooren[#], S. Denorme*, T. Ernst, C. Fenouillet-Beranger, C. Jahan, D. Lafond, H. Dansas, B. Previtali, J.P. Colonna, H. Grampeix, P. Gaud, C. Mazure**, S. Deleonibus, CEA/LETI, Grenoble, France, *STMicroelectronics, Crolles Cedex, France, [#]Freescale Semiconductor, Crolles Cedex, France, **SOITEC, Bernin, France

We investigate for the first time the experimental performance of strained Silicon Directly on Insulator (sSOI) for short and narrow FDSOI NMOS transistors integrated with TiN/HfO_2 gate stack. +16% drive current improvement is reported on 25nm gate length (among the best ever reported for short substrate-induced strained devices). Through in-depth electrical characterization and mechanical simulations, transition from bi-axial to uni-axial strain is evidenced in extremely narrow sSOI channels, with a 40% mobility enhancement for 35nm wide devices thus highlighting that the strain is not lost at sub-40nm dimensions.