SESSION 2 – TAPA I
Advanced High K Metal
Gate Stacks Integration

Tuesday, June 13, 10:15 a.m.
Chairpersons: S. Biesemans, IMEC
M. Niwa, Matsushita Electric Industrial Co., Ltd.

2.1 – 10:15 a.m.

Thermally Stable N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dielectric, H.N. Alshareef, H.R. Harris, H.C. Wen, C.S. Park, C. Huffmann, K. Choi, H.F. Luan, P. Majhi, B.H. Lee, R. Jammy, D.J. Lichtenwalner*, J.S. Jur*, A.I. Kingon*, SEMATECH, Austin, TX, *North Carolina State University, Raleigh, NC

We report a thermally stable N-metal process in which surface passivation of HfSiO dielectric using thin layers of La_2O_3, deposited by either MBE or PVD, significantly shifts the metal gate effective work function toward the Si conduction band edge. Well-behaved transistors with Lg down to 70 nm have been fabricated with threshold voltage of 0.25V, mobility up to 92% of the universal SiO_2 mobility, and Tinv ~1.6 nm.

2.2 – 10:40 a.m.

Dual Metal Gates with Band-Edge Work Functions on Novel HfLaO High- *κ* Gate Dielectric, X.P. Wang[1,2], C. Shen[1,2], M.-F. Li[1,2], H.Y. Yu[3], Y. Sun[1], Y.P. Feng[1], A. Lim[1], H.W. Sik[1], A. Chin[4], Y.C. Yeo[1], P. Lo[2], D. L. Kwong[2], [1]National University of Singapore, Singapore, [2]Institute of Microelectronics, Singapore, [3]IMEC, Leuven, Belgium, [4]National Chiao-Tung University, Hsinchu, Taiwan

In this work, by using a novel HfLaO high-κ (HK) gate dielectric, we show for the first time that with a thermal budget of 1000°C, Fermi-Pinning in the HK-metal gate (MG) stack can be released. The effective metal work function (EWF) can be tuned by a wide range more than the requirement of bulk CMOSFETs, and also fits the future UTB-SOI CMOSFETs when Si body thickness is approaching 3 nm or less. As prototype examples, TaN gate with EWF ~3.9-4.4 eV and TaN/Pt gate with EWF ~5.5 eV are shown. In addition, by replacing HfO_2 with HfLaO, high κ value and low gate tunneling are maintained, BTI Vth instability is improved by one order. These new findings are correlated to the enhanced thermal stability and significantly reduced oxygen vacancy density in HfLaO compared to HfO_2 as estimated by the first-principles calculations.

2.3 – 11:05 a.m.

Advanced Dual Metal Gate MOSFETs with High-*k* Dielectric for CMOS Application, P.F. Hsu, Y.T. Hou, F.Y. Yen, V.S. Chang, P.S. Lim, C.L. Hung, L.G. Yao, J.C. Jiang, H.J. Lin, J.M. Chiou, K.M. Yin, J.J. Lee, R.L. Hwang, Y. Jin, S.M. Chang, H.J. Tao, S.C. Chen, M.S. Liang, T.P. Ma*, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, *Yale University, New Haven, CT

This paper reports the fabrication of MOSFETs with dual metal gate electrodes. Low threshold voltage (Vt) was achieved using TaC for nFETs and MoNx for pFETs. The transistors show excellent Ion-Ioff performance with well-controlled short channel effects. Benefited from a novel approach in base oxide formation, high mobility at ~90% of poly/SiO_2 was achieved on thick HfO_2 (30A). Improvement in current drivability by the incorporation of conventional cap stressor was also presented. The data demonstrates one of the best MOSFETs to date with dual metal gates on high-k dielectrics. It is further observed that high-k crystallization induces Vt non-uniformity in small devices. To our knowledge, the impact of crystallization to high-k manufacturability is addressed here for the first time.

2.4 – 11:30 a.m.

Highly Manufacturable 45nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration, S.C. Song, Z.B. Zhang, M.M. Hussain, C. Huffman, J. Barnett, S.H. Bae, H.J. Li, P. Majhi, C.S. Park, B.S. Ju, H.K. Park, C.Y. Kang*, R. Choi, P. Zeitzoff, H.H. Tseng, B.H. Lee, R. Jammy, SEMATECH, Austin, TX, *GIST, Korea

This paper reports the first demonstration of dual high-k and dual metal gate (DHDMG) CMOSFETs meeting the device targets of 45nm low stand-by power (LSTP) node. This novel scheme has several advantages over the previously reported dual metal gate integration, enabling the high-k and metal gate processes to be optimized separately for N and PMOSFETs in order to maximize performance gain and process controllability. The proposed gate stack integration results in a symmetric short channel Vt of ~ ±0.45V with >80% high field mobility for both N and PMOSFETs and significantly lower gate leakage compared to poly/SiON stack.