SESSION 5 – TAPA II
Advanced Dynamic Memory

Tuesday, June 13, 1:30 p.m.
Chairpersons: L. Tran, Micron Technology
R. Yamada, Hitachi, Ltd.

5.1 – 1:30 p.m.
Highly Scalable Saddle-Fin(S-Fin) Transistor for Sub-50nm DRAM Technology, S.-W. Chung, S.-D. Lee, S.-A. Jang, M.-S. Yoo, K.-O. Kim, C.-O. Chung, S.Y. Cho, H.-J. Cho, L.-H. Lee, S.-H. Hwang, J.-S. Kim, B.-H. Lee, H.G. Yoon, H.-S. Park, S.-J. Baek, Y.-S. Cho, N.-J. Kwak, H.-C. Sohn, S.-C. Moon, K.-D. Yoo, J.-G. Jeong, J.-W. Kim, S.-J. Hong, S.-W. Park, Hynix Semiconductor Inc., Kyoungki-Do, Korea

Highly scalable saddle-fin cell transistor(S-Fin) has been successfully developed by combining FinFET with recess channel array transistor(RCAT). The S-Fin is simply integrated by dry-etching techniques and the desirable threshold voltage is easily obtained. The S-Fin exhibits feasible transistor characteristics such as excellent short channel effect, driving current, and refresh characteristics as compared with both RCAT and damascene-FinFET. We suggest the S-Fin is a very promising transistor structure for the sub-50nm DRAM technology.

5.2 – 1:55 p.m.
A Full FinFET DRAM Core Integration Technology Using a Simple Selective Fin Formation Technique, M. Yoshida, J. Kahng, C. Lee, S.-M. Jang, H. Sung, K. Kim, H.-J. Kim, K.-H. Jung, W. Yang, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyunggi-Do, Korea

A full FinFET DRAM core which consists of McFETs for both the sense amplifiers and the sub-word drivers, as well as FinFETs for the memory cell array has been developed. It will efficiently shrink chip size and improve chip performance, and therefore, meet requirements for the future DRAMs with 55nm or smaller design rule. Newly developed schemes which are a selective STI SiN liner removal process, a selective TiN gate stack and narrow active pitch patterning have been successfully integrated.

5.3 – 2:20 p.m.
Vertex Channel Field Effect Transistor (VC-FET) Technology Featuring High Performance and Highly Manufacturable Trench Capacitor DRAM, M. Kido, M. Kito, R. Katsumata, M. Kondo, S. Ito, K. Matsuo*, K. Miyano*, I. Mizushima*, M. Sato, H. Tanaka, H. Yasutake, Y. Nagata**, T. Hoshino^, N. Aoki, H. Aochi, A. Nitayama, Toshiba Corporation , Semiconductor Company, Kanagawa, Japan, * SoC Research & Development Center and Process & Manufacturing Engineering Center, Kanagawa, Japan, **Toshiba Information Systems Corporation, Kanagawa, Japan, ^Toshiba Microelectronics Corporation, Kanagawa, Japan

Vertex channel (VC) transistor is applied to both support devices and array transistor of trench capacitor DRAM for the first time. On-current of VC-FETs is much higher than that of conventional planar devices with keeping sufficiently small off-current. They achieve 15% or much smaller propagation delay (Tpd) of fan-out 3 than planar devices. Furthermore, 1.6 times of on-current as a planar array transistor is achieved by the combination of VCAT and P+poly gate without degradation of retention characteristics.

5.4 – 2:45 p.m.
Development of New TiN/ZrO_2/Al_2O_3/ZrO_2/TiN Capacitors Extendable to 45nm Generation DRAMs Replacing HfO_2 based Dielectrics, D.-S. Kil, H.-S. Song, K.-J. Lee, K. Hong, J.-H. Kim, K.-S. Park, S.-J. Yeom, J.-S. Roh, N.-J. Kwak, H.-C. Sohn, J.-W. Kim, S.-W. Park, Hynix Semiconductor Inc., Kyoungki-Do, Korea

New ZrO_2/Al_2O_3/ZrO_2(ZAZ) dielectric film was theoretically designed and successfully demonstrated to be applicable to 45nm DRAM devices. ZAZ dielectric film is a combined structure from tetragonal ZrO_2 and amorphous Al_2O_3. Thus prepared ZAZ TIT capacitors showed very small Tox.eq value of 6.3Å and low leakage current less than 1fA/cell. It was also confirmed that ZAZ TIT capacitor was thermally robust during backend full thermal process by applying it to the final DRAM product in mass production.