2012 Symposium on VLSI Technology Short Course
Tapa 1 and 2

14nm CMOS Technology & Design Co-Optimization and Emerging Memory Technologies

Monday, June 11

Co-chairs: M. Khare, IBM
M. Hane, Renesas

8:10 a.m. – Introduction

8:15 a.m. FinFET – History Fundamentals and Future, T-J King Liu , UC Berkeley, USA

9:25 a.m. FinFET Design Enablement – Foundry Perspective, B. Sheu,TSMC, Taiwan

10:35 a.m. Break

10:50 a.m. Heterogeneous CMOS Integration, S. Takagi , Univ. of Tokyo, Japan

12:00 p.m. Lunch

1:30 p.m. Interconnect Technology (Design, Reliability & RC), M. Angyal , IBM, USA

2:40 p.m. Break

2:55 p.m. Advanced Patterning (Design Perspective) , H. Levinson, GLOBALFOUNDRIES, USA

4:05 p.m. Emerging Memory Technology, G. H. Koh, Samsung, Korea

5:15 p.m. Conclusion

SESSION 1 – TAPA 1 / 2

Plenary Session

Tuesday, June 12, 8:05 a.m.
Chairs: K. Schruefer, Intel Mobile Communications
T. Hiramoto, The University of Tokyo

8:05 a.m. **Welcome, Opening Remarks and Awards**
M-R Lin, GLOBALFOUNDRIES
H. Wakabayashi, Sony Corp.

1.1 – 8:40 a.m.
Peering through the Technology Scaling Fog (Invited), M. Mayberry, Director of Component Research, Intel

1.2 – 9:25 a.m.
Wearable Sensing Systems for Healthcare Monitoring (Invited), I. Yamada, G. Lopez, University of Tokyo

Session 2 – TAPA 2

Advanced Fin FET Devices and Technology

Tuesday, June 12, 10:25 a.m.
Chairs: G. Yeap, Qualcomm
M. Masahara, Nat'l Institute of AIST

2.1 - 10:25 a.m.
10nm-Diameter Tri-Gate Silicon Nanowire MOSFETs with Enhanced High-Field Transport and V_{th} Tunability through Thin BOX, M. Saitoh, K. Ota, C. Tanaka, K. Uchida*, T. Numata, Toshiba Corp., *Tokyo Institute of Technology

We demonstrate high-performance 10nm-diameter tri-gate nanowire transistors (NW Tr.) with Vth tunability, small variability and negligible self-heating. Optimized S/D and stress memorization technique (SMT) lead to significant parasitic resistance reduction and mobility enhancement. Saturation velocity increase by SMT further enhances high-field carrier velocity and Ion of 1mA/um at Ioff of 100nA/um is achieved. We also demonstrate Vth control in tri-gate NW Tr. with thin BOX for the first time. The degradation of body effect by NW narrowing can be recovered by thinning NW height, enabling dynamic power and performance management.

2.2 - 10:50a.m.
Strain-Induced Performance Enhancement of Tri-Gate and Omega-Gate Nanowire FETs Scaled Down to 10nm Width, R. Coquand*, M. Cassé, S. Barraud, P. Leroux, D. Cooper, C. Vizioz, C. Comboroure*, P. Perreau, V. Maffini-Alvaro, C. Tabone, L. Tostie, F. Allain S. Barnola, V. Delaye, F. Aussenac, G. Reimbold, G. Ghibaudo**, D. Munteanu, S. Monfray*, F. Boeuf, O. Faynot, T. Poiroux,CEA-LETI, MINATEC, *STMicroelectronics, **IMEP-LAHC

A detailed study of performance in uniaxially-strained Si nanowire (NW) transistors fabricated by lateral strain relaxation of biaxial SSOI substrate is presented. 2D strain imaging demonstrates the lateral strain relaxation resulting from nanoscale patterning. For the first time, an improvement of electron mobility in SSOI NW scaled down to 10nm width has been successfully demonstrated (+55% with respect to SOI NW). This improvement is maintained even by using H2 annealing used for Omega-Gate. On short gate length, a strain-induced Ion gain as high as 40% at LG=45nm is achieved for multiple-NWs active pattern.

2.3 - 11:15a.m.

Channel Doping Impact on FinFETs for 22nm and Beyond, C.-H. Lin, R. Kambhampati*, R. Miller*, T. Hook, A. Bryant, W. Haensch, P. Oldiges, I. Lauer, T. Yamashita, V. Basker, T. Standaert, K. Rim, E. Leobandung, H. Bu, M. Khare, IBM Research Division, *GLOBALFOUNDRIES

The natural choice to achieve multiple threshold voltages (Vth) in fully-depleted devices is by choosing the appropriate gate workfunction for each device. However, this comes at the cost of significantly higher process complexity. The absence of a body contact in FinFETs and insensitivity to back-gate bias leaves the conventional channel doping approach as the most practical technique to achieve multiple Vth. This choice, however, introduces a variable that is usually not considered in the context of fully depleted devices. For the first time, we demonstrate a multiple Vth solution at relevant device geometries and gate pitch for the 22nm node. We investigated the impact of FinFET channel doping on relevant device parameters such as Tinv, mobility, electrostatic control and Vth mismatch. We also show that Vth extraction by the "constant current" method could mislead the DIBL analysis of devices with greatly different channel mobility.

2.4 - 11:40 a.m.

FinFET Parasitic Resistance Reduction by Segregating Shallow Sb, Ge and As Implants at the Silicide Interface, C. Kenney, K.-W. Ang, K. Matthews, M. Liehr, M. Minakais, M. Rodgers*, V. Kaushik*, S. Novak*, S. Gausepohl*, C. Hobbs, P. Kirsch, R. Jammy, J. Pater, SEMATECH, *CNSE State University of New York

A new contact technology comprising antimony (Sb) co-implantation and segregation to reduce Schottky barrier height (SBH) and parasitic series resistance for N-FinFETs is reported. Experiments with shallow Sb, Ge and As co-implantation in the source/drain (S/D) regions of SOI FinFET structures found that all three implant species significantly reduced extrinsic resistance. The Sb implant with a 5e13 cm-2 dose produced the best results with a 31% reduction of extrinsic resistance and a corresponding Ion increases of 19%. This optimum Sb implant is shown to reduce specific contact resistivity (ρc) by decreasing the SBH and increasing the barrier steepness. Electrostatic control comparable to the reference device indicates no degradation in short channel effects for either Sb, Ge or As.

Session 3 – TAPA 2

NAND Flash

Tuesday, June 12, 10:25 a.m.

Chairs: J. Alsmeier, SanDisk
H.-T. Lue, Macronix International Co, Ltd.

3.1 - 10:25 a.m.

A New Metal Control Gate Last Process (MCGL Process) for High Performance DC-SF (Dual Control Gate with Surrounding Floating Gate) 3D NAND Flash Memory, Y. Noh, Y. Ahn, H. Yoo, B. Han, S. Chung, K. Shim, K. Lee, S. Kwak, S.Shin, I. Choi, S. Nam, G. Cho, D. Sheen, S. Pyi, J. Choi, S. Park, J. Kim, S. Lee, S. Aritome, S. Hong, S. Park, Hynix Semiconductor Inc.

A new Metal Control Gate Last process (MCGL process) has been successfully developed for the DC-SF (Dual Control gate with Surrounding Floating gate cell)[1] three-dimensional (3D) NAND flash memory. The MCGL process can realize a low resistive tungsten (W) metal word-line with high-k IPD, a low damage on tunnel oxide/IPD, and a preferable FG shape.

And also, a conventional bulk erase can be used, replaced GIDL erase in BiCS[3][4], due to direct connection between channel poly and p-well by the channel contact holes. Therefore, by using MCGL process, high performance and high reliability of DC-SF cell can be achieved for MLC/TLC 256Gb/512Gb 3D NAND flash memories

3.2 - 10:50 a.m.
Intrinsic Fluctuations in Vertical NAND Flash Memories, E. Nowak, J.-H. Kim, H.Y. Kwon, Y.-G. Kim, J.S. Sim, S.-H. Lim, D.S. Kim, K.-H. Lee, Y.-K. Park, J.-H. Choi, C. Chung, Samsung Electronics Co. Ltd.

Vertical NAND (VNAND) technology relies on polysilicon for channel material. Two intrinsic variation sources of the cell threshold voltage induced by polysilicon traps have been identified and simulated: Random Trap Fluctuation (RTF) and Random Telegraph Noise (RTN). We demonstrate that RTN is enhanced by the polysilicon material and an original model explains the asymmetric RTN distribution observed after endurance. This work enables the prediction of VT distribution for VNAND devices in MLC operation.

3.3 - 11:15 a.m.
A New GIDL Phenomenon by Field Effect of Neighboring Cell Transistors and its Control Solutions in Sub-30 nm NAND Flash Devices, I.H. Park, W.-G. Hahn, K.-W. Song, K.H. Choi, H.-K. Choi, S.B. Lee, C.-S. Lee, J.H. Song, J.M. Han, K.H. Kyoung, Y.-H. Jun, Samsung Electronics

Gate induced drain leakage (GIDL) is one of the major mechanism which degrades program disturbances in NAND flash operations. In this study, we have observed GIDL phenomenon in scaled NAND string, such as the location or the mechanism related with band-to-band-tunneling generation, are quite different from conventional ones in sub-30 nm technologies due to the short distance between neighboring cells and lightly doped S/D region. By device simulation, we have found that the GIDL current of NAND is strongly influenced by 5-terminal biasing condition of adjacent cells and hence should be described by 5-terminal field effect model instead of conventional 3-terminal model. By silicon measurements (with a 27-nm NAND product), we have confirmed the confidence of the proposed model. The proposed model is expected to provide an important clue for making inhibit control solutions against program disturbance in sub-30 nm NAND flash devices.

3.4 - 11:40 a.m.
Ferroelectricity in HfO_2 Enables Nonvolatile Data Storage in 28 nm HKMG, J. Müller, E. Yurchuk*, T. Schlösser**, J. Paul, R. Hoffmann, S. Müller*, D. Martin*, S. Slesazeck*, P. Polakowski, J. Sundqvist, M. Czernohorsky, K. Seidel, P. Kücher, R. Boschke**, M. Trentzsch**, K. Gebauer**, U. Schröder*, T. Mikolajick*, Fraunhofer Center Nanoelectronic Technologies, *NaMLab GmbH, **GLOBALFOUNDRIES

Even though researched for several decades, the ferroelectric field effect transistor (FeFET) based on traditional perovskite-based ferroelectrics like PZT or SBT still has fundamental shortcomings. Its potential, however, remains unchallenged. Unlike the current-based STT-MRAM, RRAM, PCRAM and Flash technologies the ferroelectric approach is based on a field effect and consumes the lowest power during switching. Scalability and manufacturability on the other hand still remain a major issue when utilizing perovskite-based ferroelectrics. With the ability to engineer ferroelectricity in the well-known and fully CMOS-compatible HfO2 based dielectrics we are able to report, that the two order of magnitude scaling gap, prevailing ever since the introduction of FeFETs, has been closed at the 28 nm node. The world´s most aggressively scaled FeFETs were successfully fabricated using ferroelectric Si:HfO2 in a 28 nm HKMG stack (TiN/Si:HfO2/SiO2/Si). Excellent yield, fast switching, good retention and endurance will be demonstrated.

Session 4 – TAPA 1
High-K / Metal Gate Scaling

Tuesday, June 12, 1:30 p.m.
Chairs: T.-J. King Liu, Univ. of California, Berkeley
Y. Akasaka, Tokyo Electron Taiwan, Ltd.

4.1 - 1:30 p.m.
Implementing Cubic-Phase HfO_2 with K-Value ~ 30 in Low-V_T Replacement Gate pMOS Devices for Improved EOT-Scaling and Reliability, L.-Å. Ragnarsson, C. Adelmann, Y. Higuchi, K. Opsomer, A. Veloso, S.A. Chew, E. Röhr, E. Vecchio, X. Shi, K. Devriendt, F. Sebaai, T. Kauerauf, M. Pawlak, T. Schram, S. Van Elshocht, N. Horiguchi, A. Thean, Imec

Higher k-value HfO_2 (k~30) was evaluated in replacement metal gate pMOS devices. The higher-k was achieved by doping and anneal of the HfO_2 causing crystallization into the cubic phase. The resulting gate-stack has up to 1000 x lower gate-leakage current compared to a reference HfO_2: JG at -1 V is 2 µA/cm2 at EOT~9.7 Å. The better JG – EOT-scaling, result in performance and reliability improvements when normalized to the JG.

4.2 - 1:55 p.m.

A Novel Low Resistance Gate Fill for Extreme Gate Length Scaling at 20nm and Beyond for Gate-Last High-k/Metal Gate CMOS Technology, U. Kwon, K. Wong, S. Krishnan, L. Economikos, X. Zhang*, C. Ortolland, L.D. Thanh*, J.-B. Laloe*, J.Y. Huang*, L. Edge, H.M. Wang*, M. Gribelyuk, D. Rath*, R. Bingert**, Y. Liu*, R. Bao, I. Kim^, R. Ramachandran, W. Lai, J. Cutler, D.S. Salvador*, Y. Zhang*, J. Muncy, B. Paruchuri^^, M. Krishnan[#], V. Narayanan[#], R. Divakaruni, X. Cheng, M. Chudzik, IBM Microelectronics Division, *GLOBALFOUNDRIES, Inc., **STMicroelectronics, ^Samsung Electronics, ^^IBM Research, [#]IBM TJ Watson Research Center

Replacement metal gate (RMG) process requires gate fill with low resistance materials on top of work function tuning metals. Conventional titanium (Ti)-aluminum (Al) based RMG metal fill scheme for low resistance gate formation becomes challenging with further gate length scaling for 20nm node and beyond. In this work, we have demonstrated competitive low resistance gate formation at smaller than 25nm Lgate using a novel cobalt (Co)-aluminum based metal fill scheme for extreme gate length scaling. Challenges in CMP for the implementation as well as assessment on resistance and device characteristics of this new low resistance fill scheme are also discussed.

4.3 - 2:20 p.m.

Dramatic Improvement of High-K Gate Dielectric Reliability by Using Mono-Layer Graphene Gate Electrode, J.K. Park, S.M. Song, J.H. Mun, B.J. Cho, KAIST

We demonstrate for the first time that the high-k gate dielectric reliability is dramatically improved by replacing metal gate electrode with graphene gate electrode. The atomic-scale thickness and flexible nature of graphene completely eliminate mechanical stress in the high-k gate dielectric, resulting in significant reduction of trap generation in the high-k film. Almost all the electrical properties related to reliability of MOSFET such as the PBTI, TDDB, leakage current, etc are significantly improved. Data retention and program/erase properties of charge trap Flash memory are also greatly improved.

4.4 - 2:45 p.m.

Process Control & Integration Options of RMG Technology for Aggressively Scaled Devices, A. Veloso, Y. Higuchi, S. Chew, K. Devriendt, L. Ragnarsson, F. Sebaai, T. Schram, S. Brus, E. Vecchio, K. Kellens, E. Röhr, G. Eneman, E. Simoen, M. Cho, V. Paraschiv, Y. Crabbe, X. Shi, H. Tielens, A. Van Ammel, H. Dekkers, P. Favia, J. Geypen, H. Bender, A. Phatak*, J. Del Agua Borniquel*, K. Xu*, M. Allen*, C. Liu*, T. Xu*, W. Yoo**, A. Thean, N. Horiguchi, IMEC, *Applied Materials, **WaferMasters Inc.

We report on aggressively scaled RMG-HKL devices, with tight low-VT distributions [29mV sigma(VTsat) for PMOS, 49mV sigma(VTsat) for NMOS at 35nm Lgate] achieved through controlled EWF-metal alloying for NMOS, and providing an in-depth overview of its enabling features: 1) physical mechanisms, model supported by TCAD simulations and analysis techniques such as TEM, EDS; 2) process optimizations implementation: oxygen sources reduction, control of RF-PVD TiAl/TiN ratio and reduced Hgate, also impacting stress induced in the channel. Additional key features: 1) Al vs. W as fill-metal, with careful liner/barrier materials selection and tuning yielding well-behaved devices with tight Rgate distributions down to 20nm Lgate, and enabling both PMOS and NMOS low-VT values for high aspect-ratio gates (60nm Hgate, Lgate down to 30nm); 2) wet-etch vs. siconi clean for dummy-dielectric removal, with HfO_2 post-deposition N_2-anneal resulting in substantial BTI improvement without EOT or low-field/peak mobility penalty, and good noise response.

Session 5 – TAPA 2

Alternative Memory

Tuesday, June 12, 1:30 p.m.
Chairs: K. Attenborough, NXP Central R&D
S. Choi, Samsung Electronics Co., Ltd.

5.1 - 1:30 p.m.
Scalable 3-D Vertical Chain-Cell-Type Phase-Change Memory with 4F^2 Poly-Si Diodes, M. Kinoshita, Y. Sasago, H. Minemura, Y. Anzai, M. Tai, Y. Fujisaki, S. Kusaba, T. Morimoto, T. Takahama, T. Mine, A. Shima, Y. Yonamoto, T. Kobayashi, Hitachi, Ltd.

A scalable 3-D VCCPCM with 4F2 poly-silicon diode was fabricated and successfully demonstrated set, reset, and reading operation. Implementing this PCM device can reduce bit cost compared to flash memory.

5.2 - 1:55 p.m.
Varistor-type Bidirectional Switch (J_{MAX}>10^{7}A/cm^2, Selectivity~10^4) for 3D Bipolar Resistive Memory Arrays, W. Lee, J. Park, J. Shin, J. Woo, S. Kim, G. Choi, S. Jung, S. Park, D. Lee, E. Cha, H.D. Lee*, S.G. Kim*, S. Chung*, H. Hwang, Gwangju Institute of Science and Technology, *Hynix Semiconductor Inc.

We demonstrate a varistor-type bidirectional switch (VBS) with excellent selection property for future 3D bipolar resistive memory array. A highly non-linear VBS showed superior performances including high current density (>3x107A/cm2) and high selectivity (~104). The non-linear I-V characteristics can be explained by varistor-type multi-layer tunnel barriers, which were formed by Ta incorporation into thin TiO2. Furthermore, the 1S1R device showed excellent suppression of leakage current (>104 reduction) at 1/2VREAD, which is promising for ultra-high density resistive memory applications.

5.3 - 2:20 p.m.
Nonvolatile 32x32 Crossbar Atom Switch Block Integrated on a 65 nm CMOS Platform, N. Banno, M. Tada, T. Sakamoto, K. Okamoto, M. Miyamura, N.Iguchi, T. Nohisa, H. Hada, LEAP

A 32x32 crossbar complementary atom switch (CAS) block has been successfully integrated in a 65nm-node CMOS platform without degrading CMOS properties. The CAS connecting to two Cu lines at each edge is composed of a dual layered electrolyte of TiO2/polymer, which prevents Cu oxidation during the fabrication of the switch and Cu BEOL. The reduction of Cu-surface roughness and the electric field concentration at the edge of Cu electrode enable a high Ion/Ioff ratio and a low programming voltages of 1.8V with distribution as low as σ=0.2V.

5.4 - 2:45 p.m.
Large-Scale (512kbit) Integration of Multilayer-Ready Access-Devices Based on Mixed-Ionic-Electronic-Conduction (MIEC) at 100% Yield, G.W. Burr, K. Virwani, R.S. Shenoy, A. Padilla, M. BrightSky*, E.A. Joseph*, M. Lofaro*, A.J. Kellock, R.S. King, K. Nguyen, A.N. Bowers, M. Jurich, C.T. Rettner, B. Jackson, D.S. Bethune, R.M. Shelby, T. Topuria, N. Arellano, P.M. Rice, B.N. Kurdi, K. Gopalakrishnan, IBM Almaden Research Center, *IBM TJ Watson Research Center

BEOL-friendly Access Devices (AD) based on Cu-containing MIEC materials are integrated in large (512x1024) arrays at 100% yield, and are successfully co-integrated together with Phase Change Memory (PCM). Numerous desirable attributes are demonstrated: the large currents (>200uA) needed for PCM, the bipolar operation required for high-performance RRAM, the single-target sputter deposition essential for high-volume manufacturing, and the ultra-low leakage (<10 pA) and high voltage margin (1.5V) needed to enable large crosspoint arrays.

Session 6 – TAPA 1

Low Power and Steep Subthreshold Technology

Tuesday, June 12, 3:25 p.m.
Chairs: A. Seabaugh, Notre Dame Univ.
T. Iwamatsu, Renesas Electronics Corp.

6.1 – 3:25 p.m.
Recent Progress and Challenges for Relay Logic Switch Technology (Invited), T.-J. King Liu, L. Hutin, I-R. Chen, R. Nathanael, Y. Chen, E. Alon, University of California, Berkeley

The energy efficiency of CMOS technology is fundamentally limited by transistor off-state leakage (Ioff). Mechanical switches have zero Ioff and therefore could be advantageous for ultra-low-power digital logic applications. This paper discusses recent advancements in relay logic switch technology and current challenges which must be addressed to realize its promise.

6.2 – 3:50 p.m.
III-V Field Effect Transistors for Future Ultra-Low Power Applications (Invited), G. Dewey, B.C. Kung, R. Kotlyar, M. Metz, N. Mukherjee, M. Radosavljevic, Intel Corp.

This paper summarizes the electrostatics and performance of III-V field effect transistors including thin body planar MOSFETs, 3-D tri-gate MOSFETs, and Tunneling FETs (TFETs). The electrostatics of the III-V devices is shown to improve from thick body planar to thin body planar and then to 3-D tri-gate. Beyond the MOSFET structures, sub-threshold slope (SS) steeper than 60 mV/decade has been demonstrated in III-V TFETs. These III-V devices, especially the 3-D tri-gate MOSFET and TFET, are viable options for future ultra low power applications.

6.3 – 4:15 p.m.
Steep-Slope Tunnel Field-Effect Transistors Using III-V Nanowires/Si Heterojunction (Invited), K. Tomioka, M. Yoshimura, T. Fukui, Hokkaido University

In this paper, we report on a tunneling field-effect transistors (TFETs) using III-V nanowire (NW)/Si heterojunctions. We experimentally demonstrate steep turn-on behaviors using the TFET with surrounding-gate architecture and high-*k* dielectrics. Adjusting series resistances in this device structure is important for achieving steep-slope switching. A minimum subthreshold slope (SS) of the TFET is 21 mV/dec (V_{DS} of 0.10 – 1.00 V) at room temperature.

6.4 - 4:40 p.m.
Strained Tunnel FETs with Record Ion:First Demonstration of ETSOI TFETs with SiGe Channel and RSD, A. Villalon, C. Le Royer, M. Cassé, D. Cooper, B. Prévitali, C. Tabone, J.-M. Hartmann, P. Perreau, P. Rivallin, J.-F. Damlencourt, F. Allain, F. Andrieu, O. Weber, O. Faynot, T. Poiroux, CEA, LETI, Minatec

We present for the first time Tunnel FETs (TFETs) obtained with a FDSOI CMOS process flow featuring High-K Metal Gate, ultrathin body compressively strained SiGe (Ge content from 0 to 30%) based channels, and SiGe30% Raised SD. We analyse the tunnelling improvements due to the different technological injection boosters: ultrathin body & EOT, strain, low band gap source, and low temperature SD anneal. For the first time, TFETs with large ON current (up to 428µA/µm) are demonstrated (with >x1000 ION gain vs. SOI reference).

6.5 - 5:05 p.m.
Demonstration of Improved Heteroepitaxy, Scaled Gate Stack and Reduced Interface States Enabling Heterojunction Tunnel FETs with High Drive Current and High On-Off Ratio, D. Mohata, B. Rajamohanan, Y. Zhu*, M. Hudait*, R. Southwick*, Z. Chbili**, D. Gundlach**, J. Suehle**, J. Fastenau^, D. Loubychev^, A. Liu^, T. Mayer, V. Narayanan, S. Datta, The Pennsylvania State University, *Virginia Tech, **NIST, ^IQE Inc.

Staggered tunnel junction (GaAs0.35Sb0.65 /In0.7Ga0.3As) is used to demonstrate heterojunction tunnel FET (TFET) with the highest drive current, Ion, of 135µA/µm and highest Ion/Ioff ratio of 2.7 □104 (Vds=0.5V, Von-Voff=1.5V). Effective oxide thickness (EOT) scaling (using Al2O3/HfO2 bilayer gate stack) coupled with pulsed I-V measurements (suppressing Dit response) enable demonstration of steeper switching TFET.

Session 7 – TAPA 2

STT MRAM

Tuesday, June 12, 3:25 p.m.

Chairs: E. Kan, Cornell Univ.
S. Hong, Hynix Semiconductor, Inc.

7.1 - 3:25 p.m.

Enhancement of Data Retention and Write Current Scaling for Sub-20nm STT-MRAM by Utilizing Dual Interfaces for Perpendicular Magnetic Anisotropy, J.-H. Park, Y. Kim, W. Lim, J. Kim, S. Park, J. Kim, W. Kim, K. Kim, J. Jeong, K.S. Kim, H. Kim, Y.J. Lee, S. Oh, J.E. Lee, S.O. Park, S. Watts*, D. Apalkov*, V. Nikitin*, M. Krounbi*, S. Jeong, S. Choi, H. Kang, C. Chung, Samsung Electronics Co., Ltd., *Grandis Inc.

We investigate the sub-20nm level scalability of STT-MRAM cells possessing perpendicular magnetization induced from the interface of free layer (FL) and MgO tunnel barrier. We demonstrate that the MTJs utilizing dual interfaces of FL and MgO exhibit enhanced scalability with high thermal stability and low switching current, compared with the MTJs with a single interface. As thermal stability factor (delta) varies as a function of MTJ dimension, MTJs with dual interfaces show over 60 at 20nm node, while MTJs of single interface show around 33. MTJs with dual interface also exhibit lower switching current per thermal stability (Ic/delta), ~1/2 level of single interface MTJs.

7.2 - 3:50 p.m.

Demonstration of Non-Volatile Working Memory Through Interface Engineering in STT-MRAM, C. Yoshida, T. Ochiai, Y. Iba, Y. Yamazaki, K. Tsunoda, A. Takahashi, T. Sugii, LEAP

We engineered the interface of the MgO barrier prepared by post-oxidation of Mg metal to improve structural and electronic properties of magnetic tunnel junctions (MTJs). Drastic improvements in magnetoresistance ratio (MR) and critical switching voltage (Vc) with low resistance area product (RA) were achieved by inserting CoFe seed layer under the oxidized barrier. The MTJ satisfied over 1016 write cycles at 10 ns pulse under the operation voltage of 0.65 V. From these results, we have verified for the first time the hypothesis that a spin transfer torque magnetoresistance random access memory (STT-MRAM) is suitable for a non-volatile working memory.

7.3 - 4:15 p.m.

High-speed and Reliable Domain Wall Motion Device: Material Design for Embedded Memory and Logic Application, S. Fukami, M. Yamanouchi, T. Koyama*, K. Ueda*, Y. Yoshimura*, K.J. Kim*, D. Chiba*, H. Honjo**, N. Sakimura**, R. Nebashi**, Y. Kato**, Y. Tsuji**, A. Morioka**, K. Kinoshita, S. Miura**, T. Suzuki^, H. Tanigawa^, S. Ikeda, T. Sugibayashi**, N. Kasai, T. Ono, H. Ohno, Tohoku University, *Kyoto University, **NEC Corp., ^Renesas Electronics Corp.

High-speed capability and excellent reliability of a magnetic domain wall (DW) motion device required for high-speed embedded memory and logic-in-memory applications were achieved by optimizing the film stack structure of Co/Ni wire. Low-current with high-speed writing, high heat resistance, low error rate, wide operation range for temperature and magnetic field, high retention, and high endurance features were confirmed. The developed technology here makes an ultra-low-power system LSI possible.

7.4 - 4:40 p.m.

Spintronics Primitive Gate with High Error Correction Efficiency 6 $(P_{error})^2$ for Logic-in Memory Architecture, Y. Tsuji, R. Nebashi, N. Sakimura, A. Morioka, H. Honjo, K. Tokutome, S. Miura, T. Suzuki*, S. Fukami*, K. Kinoshita^, T. Hanyu^, T. Endo^, N. Kasai^, H. Ohno^, T. Sugibayashi, NEC Corp., *Renesas Electronics Corp., ^Tohoku University

A spintronics primitive gate with redundancy was designed using domain wall motion (DWM) cells, and the data-missing rate was drastically improved to ~ 6 (Perror)^2 when the error rate per DWM cell was (Perror). All the DW motion cells aligned in series were written simultaneously, which suppressed the increase in power consumption when writing. Application of 4-terminal DWM cells with physically separated current paths for writing and reading saved extra path transistors for redundancy and there were no area overheads.

7.5 - 5:05 p.m.
Highly Scalable STT-MRAM with 3-Dimensional Cell Structure Using In-plane Magnetic Anisotropy Materials, S. Lee, K. Kim, K. Kim, U. Pi, Y. Jang, U.-I. Chung, I. Yoo, K. Kim, SAIT

Novel spin transfer torque MRAM cells with three dimensional freelayer structures were suggested for the high density memory below 20nm technology node. By folding the freelayer to a special geometry, the 3D MTJ Cell structure retains large freelayer volume without an increase of cell foot-print, scaling down the MRAM cells even with in-plane magnetic anisotropy materials. From the micromagnetic calculation with Nudged Elastic Band (NEB) method, we confirmed the thermal stability over 60 in 3D MTJ cell with 15 x 30nm2 area.

Technology Rump Sessions
Tuesday, June 12, 8:00 p.m. – 10:00 p.m.

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 12
8:00 p.m. – 10:00 p.m.

Organizers:

Circuits	**Technology**
M. Bauer, Micron	T. Skotnicki, STMicroelectronics
N. Lu, Etron	K. Miyashita, Toshiba

RJ1: Scaling Challenges Beyond 1x nm DRAM and NAND Flash

Moderator: R. Shrivastava, SanDisk
N. Lu, Etron

The combined revenues of DRAM and NAND Flash approached $54 Billion in 2010. This is expected to continue to grow in the coming years. Emerging silicon and package technologies will further drive lower cost and new applications. The difficulty of scaling and developing new technologies and investments to build new factories is increasing at about the same rate as the memory bit growth in the world. At the same time, the industry is becoming aware that we are closing in on physical and electrical scaling limitations. As we close in on scaling limits, the use of new materials, manufacturing processes, and circuit design will become unavoidable. To compound the problem, fierce competition is forcing shorter development times. Our industry needs to openly address these issues and challenges in order to continue developing better and lower cost memories for the decade to come. The whole industry faces these challenges and issues. They are huge. We have assembled a representative group of industry experts for this Joint Rump Session. We will ask them to discuss the top issues from the perspective of each one's area of expertise. The floor will be open to question the panelist's view or challenge them to consider issues that audience would like to raise.

Panelists:

S. Aritome, Hynix
G. Atwood, Micron

G. Bronner, Rambus
H. Hazama, Toshiba
H-K Kang, Samsung
C.Y. Lu, Macronix
M. Koyanagi, Tohoku University
K. Takeuchi, University of Tokyo

R2: Evolution of FinFET and beyond?

Moderators: G. Yeap, Qualcomm
Y. Miyamoto, Tokyo Institute of Technology

As conventional scaling approaches its limits, the semiconductor industry has been evaluating for more than a decade on 3D multi-gate FINFET/Tri-gate transistors as well as planar transistors with alternative channel designs (such as FD-SOI, Ge, III-V) for achieving the power efficiency, performance, density, reliability, and form factor required in advanced mobile devices.

It is extremely exciting that in 2012 the industry finally enters into the 3-D era with the high volume production of 3-D Tri-gate/FinFET transistors in 22nm standalone CPU technology. Did 1st generation 3-D tri-gate transistor fully deliver the power/performance value proposition, and achieve the required density/cost and reliability? How well can multi-gate 3D or alternative channel designs overcome scaling bottlenecks, such as parasitic R&C and variability? How fast the 3-D transistor production will spread to other applications especially the driver application of mobile computing SoC? Will 3-D transistor technology completely and utterly dominate the industry or there are rooms for planar architecture be extended or enhanced for a cost/PPA sweatspot for certain applications/markets? How will the 2nd/3rd generation 3-D technology look like? How best the 3-D transistor technology coupled with 2.5/3-D interconnect technology to deliver holistic system scaling for complex, power constrained mobile computing and wireless applications? What is life after FinFET – any Joker left in the pocket?

This panel moderated by Geoffrey Yeap/Y. Miyamoto will start out with a "fire side chat" on the issues from each panelist's perspective, and evolve into a what we hope is a passionate discussion with some serious audience participation. The panelists whose views range across the spectrum include:

Panelists

F. Boeuf, STMicroelectronics
J.P. Colinge, TSMC
W. Haensch, IBM
D.W. Kim, Samsung
A. Thean, imec
S. Thompson, SuVolta

R3: Advanced Patterning for Next Generation Technology Nodes: EUV or Tricky-193nm, EBDW? DSA, Resists, Masks, Regular Layouts, Metrology?

Moderators : G. Vandenberghe, IMEC
M. Tomoyasu, Tokyo Electron

To EUV or not to EUV? That is at least one of the questions that will be tackled by all panelists. In this rump session, the lithography/patterning challenges to enable further scaling will be discussed by multiple experts, involved in the many different fields of lithography as chipmaker, fabless company or equipment manufacturer. What are the ultimate limits

of 193nm immersion lithography with multiple patterning schemes? What is the manufacturability readiness of EUV lithography? And how about ebeam direct write? Can directed self assembly be seen as an extension technique? Are only unidirectional layouts allowed and how will the EDA tackle the patterning complexity? What will be the patterning demand from under layer materials and structure direction? How will the metrology enable the lithography challenges?

Y. Borodovsky, Intel
A. Chen, ASML
H. Levinson, GLOBALFOUNDRIES
B. Lin, TSMC
S. Nagahara, TEL
A. Yamaguchi, Hitachi

Session 8 – TAPA 1
RRAM I

Wednesday, June 13**,** 8:05 a.m.
Chairs: J. Zahurak, Micron Technology, Inc.
N. Kasai, Tohoku Univ.

8.1 - 8:05 a.m.
A Novel Cross Point One-Resistor (0T1R) Conductive Bridge Random Access Memory (CBRAM) with Ultra Low Set/Reset Operation Current, F.M. Lee, Y.Y. Lin, M.H. Lee, W.C. Chien, H.L. Lung, K.Y. Hsieh, C.Y. Lu, Macronix International Co., Ltd.

Using the dual Vth characteristics of a multi-layer HfO2/SiO2/Cu-GST conducting bridge (CB) structure we can construct a one-resistor cell without an access device (0T1R). Like 1T Flash memory the Vth is used to store the logic state thus leaving all devices always at high resistance state and a separate isolation device is not needed. The Vth of the cell is determined by the presence of CB in the HfO2 layer only. The CB in the SiO2 is present only temporarily during reading, and is spontaneously dissolved afterward. This spontaneous rupture of the filament in the SiO2 layer greatly reduces the switching current as well as reducing the read disturb. The mechanism for the spontaneous rupture phenomenon is investigated.

8.2 - 8:30 a.m.
Field-Driven Ultrafast sub-ns Programming in W\\Al_2O_3\Ti\CuTe-Based 1T1R CBRAM System, L. Goux, K. Sankaran, G. Kar, N. Jossart, K. Opsomer, R. Degraeve, G. Pourtois, G.-M. Rignanese*, C. Detavernier**, S. Clima, Y.-Y. Chen, A. Fantini, B. Govoreanu, D.J. Wouters, M. Jurczak, L. Altimime, J. Kittl, imec, *UCL and ETSF, **University of Gent

We optimize a 90nm-wide CuTe-based 1T1R CBRAM cell for highly controlled and ultrafast programming by engineering Al2O3 electrolyte and Ti buffer layers of appropriate density and thickness resp. By means of electrical and ab initio modeling, we demonstrate that switching is mainly controlled by field-driven motion of Cu+ species. Sub-ns programming is allowed by strong ionic-hopping barrier reduction over short insulating gap. Complete picture of conductance and switching phenomenology is shown in the entire operation range.

8.3 - 8:55 a.m.
Multi-level Switching of Triple-layered TaOx RRAM with Excellent Reliability for Storage Class Memory, S.R. Lee, Y.-B. Kim, M. Chang, K.M. Kim, C.B. Lee, J.H. Hur, G.-S. Park, D. Lee, M.-J. Lee, C.J. Kim, U.-I. Chung, I.-K. Yoo, K. Kim, Samsung Advanced Institute of Technology

A highly reliable RRAM with multi-level cell (MLC) characteristics were fabricated using a triple-layer structure (base layer/oxygen exchange layer/barrier layer) for the storage class memory applications. A reproducible multi-level switching behaviour was successfully observed, and simulated by the modulated Schottky barrier model. Morevoer, a

new programming algorithm was developed for more reliable and uniform MLC operation. As a result, more than 10^7 cycles of switching endurance and 10 years of data retention at 85C for all the 2 bit/cell operation were archieved.

8.4 - 9:20 a.m.
Conductive Filament Scaling of TaOx Bipolar ReRAM for Long Retention with Low Current Operation, T. Ninomiya, T. Takagi, Z. Wei, S. Muraoka, R. Yasuhara, K. Katayama, Y. Ikeda, K. Kawai, Y. Kato, Y. Kawashima, S. Ito, T. Mikawa, K. Shimakawa, K.Aono, Panasonic Corporation

We demonstrate for the first time that the density of oxygen vacancy in a conductive filament plays a key role in ensuring data retention. We achieve very good retention results up to 100 hours at 150˚C even under the low current operation due to the scaling of conductive filament size while retaining sufficiently high density of oxygen vacancy.

8.5 - 9:45 a.m.
Dynamic 'Hour Glass' Model for SET and RESET in HfO_2 RRAM, R. Degraeve, A. Fantini, S. Clima, B. Govoreanu, L. Goux, Y.Y. Chen, D. Wouters, P. Roussel, G.S. Kar, G. Pourtois, S. Cosemans, J. Kittle, G. Groeseneken, M. Jurczak, L. Altimime, IMEC

The set and reset process in HfO2 RRAM filament is modeled as a dynamic flow between two oxygen vacancy reservoirs connected by a narrow filament. The current is controlled by the width of the filament, that determines the electron transmission. The diffusion of oxygen vacancies is controlled by the local power in the filament. As a result, RESET is modeled as a dynamic balance between an upward and downward vacancy flow, while SET is modeled as an unbalanced filament growth bounded by the external compliance.

Session 9 – TAPA 2
Process Technology

Wednesday, June 13, 10:25 a.m.
Chairs: C.-P. Chang, Applied Materials
K. Miyashita,Toshiba Corp.

9.1 - 10:25 a.m.
Atom Probe Tomography for 3D-Dopant Analysis in FinFET Devices, A.K. Kambham, G. Zschaetzsch, Y. Sasaki, M. Togo, N. Horiguchi, J. Mody, A. Florakis, D.R. Gajula*, A. Kumar, M. Gilbert, W. Vandervorst, imec, *Gueen's University of Belfast

As the nano scale device performance depends on the detailed engineering of the dopant distribution, advanced doping processes are required. Progressing towards 3D-structures like FinFETs, studying the dopant gate overlap and conformality of doping calls for metrology with 3D-resolution and the ability to confine the analyzed volume to a small 3D-structure. We demonstrate that through an appropriate methodology this is feasible using Atom Probe Tomography (APT). We extract the 3D-dopant profile and important parameters such as gate overlap and profile steepness, from transistor formed with plasma doping processes. Analyzing samples with different doping processes, the APT results are entirely consistent with device performances (Ioff vs. Ion).

9.2 - 10:50 a.m.
A 32nm High-K and Metal-Gate Anti-Fuse Array Featuring a 1.01µm^2 1T1C Bit Cell, S. Kulkarni, S. Pae, Z. Chen, W. Hafez, B. Pedersen, A. Rahman, T. Tong, U. Bhattacharya, C.-H. Jan, K. Zhang, Intel Corporation

A 1 k-bit high-density OTP (One Time Programmable)-ROM array featuring a new anti-fuse memory is presented using 32nm high-k (HK) and metal-gate (MG) CMOS process. Our 32nm HK+MG SOC process technology enables smallest reported one-transistor one-capacitor (1T1C) bit cell area measuring 1.01µm2. The 32-row by 32-column array with a programmable sensing scheme demonstrates yield exceeding 99.9% and robust reliability.

9.3 - 11:15 a.m.
Replacement Metal Gate Extendible to 11 nm Technology, N. Yoshida, X. Fu, K. Xu, Y. Lei, H. Yang, S. Sun, H. Chen, A. Darlak, R. Donohoe, C. Lazik, R. Jakkaraju, A. Noori, S. Hung, I. Peidous, C.-P. Chang, A. Brand, Applied Materials

This paper describes Co-Al metal fill capable of filling sub-10nm trenches. Co-Al fill shows no degradation of threshold voltage (VTH) variation. The conductivity of the fill was evaluated using a Co-Al alloy conductance model. Co-Al shows extendibility to 11nm by the superior conductivity and gap fill.

9.4 - 11:40 a.m.
ZnO: An Attractive Option for n-Type Metal-Interfacial Layer-Semiconductor (Si, Ge, SiC) Contacts, P. Paramahans Manik, S. Gupta*, R.Mishra, N. Agarwal, A. Nainani*, Y.-C. Huang*, M. Abraham*, S. Kapadia, U. Ganguly, S. Lodha, Indian Institute of Technology Bombay, *Applied Materials Inc.

We propose ZnO as a highly attractive interfacial layer (IL) option for n-type metal-IL-semiconductor (Si, Ge, SiC) MIS contacts because of (i) good conduction band alignment between ZnO and Si/Ge/SiC, (ii) high n-type doping possible in ZnO, and, (iii) low Fermi-level pinning factor for metal/ZnO contacts. Device simulations suggest better scalability for MIS contacts versus silicides/germanides for future FinFET technologies. Contact diode measurements on Ti/n+ZnO/n-Ge and Ti/n+ZnO/n-Si devices show nearly 1000x increase in current densities due to the presence of an n+-ZnO IL. In comparison to alternate IL options such as Al2O3 and TiO2, n+-ZnO gives significantly higher current densities on n-Ge as demonstrated through device simulations and experimental data. Specific contact resistivity of 1x10-6 Ω cm2 is demonstrated through circular TLM devices fabricated on n+-Ge (1x1019 cm-3) substrates using n+ZnO IL.

Session 10 – TAPA 3

Technology / Circuits Joint Focus Session – Memory

Wednesday, June 13, 10:25 a.m.
Chairs: J. Zahurak, Micron Technology
M. Hane, Renesas Electronics Corp.

10.1 – 10:25 a.m.
SRAMs Design in Nano-Scale CMOS Technologies (Invited), K. Zhang, Intel Corp.

SRAM continues to serve as the workhorse of embedded memory for all modern VLSI systems. But SRAM scaling has become increasingly challenging in meeting both power and density requirements due to relentless miniaturization in the 6T SRAM cell area. Innovative circuit technologies along with key process advancement are discussed and they have been proven to be essential for the SRAM scaling to continue to follow Moore's law well into the future.

10.2 – 10:50 a.m.
Hybrid Memory Cube New DRAM Architecture Increases Density and Performance (Invited), J. Jeddeloh, B. Keeth, Micron

Multi-core processor performance is limited by memory system bandwidth. The Hybrid Memory Cube is a three-dimensional DRAM architecture that improves latency, bandwidth, power and density. Through-silicon vias (TSVs), 3D packaging and advanced CMOS performance enable a new approach to memory system architecture. This talk will cover the architecture, design methodology, TSV process challenges and trade-offs of Micron's Hybrid Memory Cube.

10.3 – 11:15 a.m.
Restructuring of Memory Hierarchy in Computing System with Spintronics-Based Technologies (Invited), T. Endoh, T. Ohsawa, H. Koike, T. Hanyu, H. Ohno, Tohoku University

The restructuring of memory hierarchies that are caught in a dilemma between performance-gain and power-reduction is one of the most promising ways to achieving the high-end and low-power computers. To this end, several possibilities of using NV memories and NV logic with STT-MTJ as levels in new hierarchies are discussed. A new NV-SRAM cell consisting of four transistors and two MTJs is shown to be a promising candidate for NV-cache memories. For NV-main

memories, we propose a PFET-based 1T-1MTJ cell. A new NV-latch that can be constructed in flip-flops of synchronous circuits is proposed and 600MHz operation is experimentally demonstrated.

10.4 - 11:40 a.m.

A Highly Pitch Scalable 3D Vertical Gate (VG) NAND Flash Decoded by a Novel Self-Aligned Independently Controlled Double Gate (IDG) String Select Transistor (SSL), C.-P. Chen, H.-T. Lue, K.-P. Chang, Y.-H. Hsiao, C.-C. Hsieh, S.-H. Chen, Y.-H. Shih, K.-Y. Hsieh, T. Yang, K.-C. Chen, C.-Y. Lu, Macronix International., Ltd.

Despite vertical stacking, the lateral scaling of 3D NAND Flash is critically important because otherwise >16 stacking layers are needed to be cost competitive to 20nm 2D NAND. In this work, we propose a 3D vertical gate (VG) NAND using a self-aligned independently controlled double gate (IDG) string select transistor (SSL) decoding method. The IDG SSL provides excellent program inhibit and read selection without any penalty of cell size increase, making our 3D VG NAND cell as scalable as conventional 2D NAND. We present the world's first < 50nm (37.5nm) half-pitch 3D NAND. The BL decoding and page operation methods are illustrated in detail. This highly pitch scalable VG with IDG SSL approach provides a very cost competitive 3D NAND.

Session 11 – TAPA 2
Mobility Enhancement

Wednesday, June 13, 1:30 p.m.

Chairs: M. Mehrotra, Texas Instruments
S. Takagi, The University of Tokyo

11.1 - 1:30pm

A New Liner Stressor (GeTe) Featuring Stress Enhancement due to Very Large Phase-Change Induced Volume Contraction for p-Channel FinFETs, R. Cheng, Y. Ding, S.M. Koh, A. Gyanathan, F. Bai, B. Liu, Y.-C. Yeo, National University of Singapore

We report the first demonstration of a novel GeTe liner stressor which exhibits very large volume contraction during phase-change, and its integration in p-channel FinFETs for strain engineering. Conformally grown GeTe liner with different thicknesses was formed on FinFETs with ultra-scaled gate length LG down to ~3 nm. When GeTe changes phase from amorphous (α-GeTe) to crystalline state (c-GeTe), GeTe liner contracts and compresses the Si source/drain region in the fin, leading to very high channel stress. Significant drive current IDsat enhancement of 69% and 106% were observed for FinFETs with 30 nm and 50 nm c-GeTe liner stressor over the control devices, respectively.

11.2 - 1:55pm

GeSn Channel nMOSFETs: Material Potential and Technological Outlook, S. Gupta, B. Vincent*, D. Lin*, M. Gunji, A. Firrincieli*, F. Gencarelli*, B. Magyari-Köpe, B. Yang**, B. Douhard*, J. Delmotte*, A. Franquet*, M. Caymax*, J. Dekoster*, Y. Nishi, K. Saraswat, Stanford University, *IMEC, **GLOBALFOUNDRIES

Semiconducting germanium tin (GeSn) alloy has recently emerged as a candidate for high performance CMOS and optoelectronic devices because of its tunable direct gap and potential for high electron and hole mobilities. High hole mobility in GeSn channel pMOSFETs has already been demonstrated. However, GeSn as channel for nMOSFETs has not yet been explored. In this work we perform detailed theoretical analysis to gauge the benefits of GeSn channel over Ge for nMOSFETs. Our analysis predicts GeSn nMOSFETs to outperform Ge. GeSn n-channel devices have been successfully fabricated and factors limiting its performance are investigated, potential solutions are presented.

11.3 - 2:20pm

Strained Germanium-Tin (GeSn) N-Channel MOSFETs Featuring Low Temperature N^+/P Junction Formation and $GeSnO_2$ Interfacial Layer, G. Han, S. Su*, L. Wang, W. Wang, X. Gong, Y. Yang, Ivana, P. Guo, C. Guo, G. Zhang*, J. Pan**, Z. Zhang**, C. Xue*, B. Cheng*, Y.-C. Yeo, National University of Singapore, *Chinese Academy of Sciences, **A*STAR

In this paper, we report the world's first germanium-tin (GeSn) channel nMOSFETs. Highlights of process module advances are: low temperature (400 ˚C) process for forming high quality n+/p junction with high dopant activation and reduced dopant diffusion; interface engineering achieved with GeSnO2 interfacial layer (IL) between high-k gate dielectric and GeSn channel. A gate-last process was employed. The GeSn nMOSFET with GeSnO2 IL demonstrates a substantially improved SS in comparison with Ge control, and an ION/IOFF ratio of 104.

11.4 - 2:45pm

Towards High Performance $Ge_{1-x}Sn_x$ and $In_{0.7}Ga_{0.3}As$ CMOS: A Novel Common Gate Stack Featuring Sub-400 ºC Si_2H_6 Passivation, Single TaN Metal Gate, and Sub-1.3 nm EOT, X. Gong, S. Su*, B. Liu, L. Wang, W. Wang, Y. Yang, E. Kong, B. Cheng*, G. Han, Y.C. Yeo, National University of Singapore, *Chinese Academy of Sciences

We report a novel common gate stack solution for Ge1-xSnx P-MOSFET and In0.7Ga0.3As N-MOSFET, featuring sub-400 ºC Si2H6 passivation, sub-1.3 nm EOT, and single TaN metal gate. Symmetric VTH, high performance, low gate leakage, negligible hysteresis, and excellent reliability were realized. Using this gate stack, the world's first GeSn short-channel device with gate length LG down to 250 nm was realized. Drive current of more than 1000 µA/µm was achieved, with peak intrinsic transconductance of ~ 465 µS/µm at VDS of -1.1 V.

Session 12 – TAPA 3

Technology / Circuits Joint Focus Session – 3D-System Integration

Wednesday, June 13, 1:30 p.m.

Chairs: A. Antonelli,Novellus Systems, Inc.
T. Tanaka, Tohoku Univ.

12.1 – 1:30 p.m.

Practical Implications of Via-Middle Cu TSV-induced Stress in a 28nm CMOS Technology for Wide-IO Logic-Memory Interconnect (Invited), J. West, Y.S. Choio, C. Vartuli, Texas Instruments

The impact of isolated and arrayed 10x60□m via-middle Cu TSVs on 8LM 28nm node CMOS poly-SiON P/NFETs was electrically measured for proximities >4 □m at 27C and 105C. The largest observed shift in I_{on} (<2.3%) is significantly less than that from other context-dependent sources such as dual stress liner boundaries (~10%). NanoBeam Diffraction measurements of Si strain within 5□m of TSVs were acquired for samples prepared from fully processed wafers, showing that for proximity >1.5□m the impact of TSVs is negligible. Interaction with overlying interconnect is mitigated through optimization of post-TSV plating anneal to achieve <200Å Cu pumping and by introducing a TSV unit cell designed to minimize the impact on local environment.

12.2 – 1:55 p.m.

Thermal Stress Characteristics and Impact on Device Keep-Out Zone for 3-D ICs Containing Through-Silicon-Vias (Invited),T. Jiang, S-K Ryu, Q. Zhao, J. Im, H-Y Son, K-Y Byun, R. Huang, P.S. Ho, University of Texas, Austin and Hynix

Thermal stresses in TSV structures have been measured using micro-Raman spectroscopy and precision wafer curvature technique as a function of temperature and during thermal cycling. The results were verified by finite element analysis (FEA) to characterize the thermal stress behavior of the TSV structures. A nonlinear stress relaxation was observed during initial heating and no preferred grain orientation was found, indicating a homogeneous Cu grain structure with no pronounced elastic anisotropy. The stress impact on the keep-out zone (KOZ) for devices near the TSVs was investigated.

12.3 – 2:20 p.m.

Near-Field Wireless Connection for 3D-System Integration (Invited), T. Kuroda, Keio University

This paper describes a near-field wireless connection using inductive coupling, namely ThruChip Interface (TCI). TCI is a digital CMOS circuit solution in a standard CMOS technology. It is much less expensive than TSV but bears comparison in performance. Aggregated data rate of 8Tb/s is achieved by arranging 1000 channels in 6.4 mm^2. Energy consumption is 0.01pJ/b. Delay and energy dissipation will scale down by device miniaturization. If chip thickness is also thinned to 1/α,

both electric field of FET and magnetic field of TCI are kept constant and aggregated data rate per area is increased by α^3 and energy per bit is reduced to $1/\alpha^3$.

12-4 - 2:45 p.m.
An Ultra-Thin Interposer Utilizing 3D TSV Technology, W.-C. Chiou, K.-F. Yang, C. Yeh, S.-H. Wang, Y.-H. Liou, T.-J. Wu, J.-C. Lin, C.-C. Hsieh, H.A. Teng, C.C. Chiu, D.C. Yeh, W.C. Wu, A.J. Su, S.L. Chiu, H.-P. Chang, J. Wei, Y.-C. Lin, Y.-H. Chen, H.-J. Tu, H.D. Ko, T.-H. Yu, J.P. Hung, P.-H. Tsai, C.L. Huang, S.W. Lu, S.Y. Hou, D.-Y. Shih, K.H. Chen, S.-P. Jeng, C.-H. Yu, TSMC

To achieve ultra small form factor package solution, an ultra-thin (50µm) Si interposer utilizing through-silicon-via (TSV) technology has been developed. Challenges associated with handling thin wafer and maintaining package co-planarity have been overcome to stack thin dies (200µm) on ultra-thin interposer. Improved electrical performance and the advantages of this innovative thin interposer are highlighted in this paper. Warpage behavior is investigated with simulation and experiments to ensure reliability and robustness of the Si stack. Reduction in package thickness is realized to achieve high functionality, small form factor, better electrical performance and robust reliability by stacking thin dies on ultra-thin interposer.

Session 13 – TAPA 2
Ultra-Thin Body Devices

Wednesday, June 13, 3:25 p.m.
Chairs: M. Khare, IBM
C.H. Wann, TSMC

13.1 - 3:25 p.m.
Poly/High-k/SiON Gate Stack and Novel Profile Engineering Dedicated for Ultralow-Voltage Silicon-on-Thin-BOX (SOTB) CMOS Operation, Y. Yamamoto, H. Makiyama, T.Tsunomura, T. Iwamatsu, H. Oda, N. Sugii, Y. Yamaguchi, T. Mizutani*, T. Hiramoto, LEAP, *University of Tokyo

We demonstrated Silicon on Thin Buried oxide (SOTB) CMOS especially designed for ultralow-voltage (ULV) operation down to 0.4 V for the first time. Utilizing i) dual-poly gate stack with high-k having quarter-gap work functions best for the ULV CMOS operation, and ii) a novel "local ground plane (LGP)" structure that significantly improves short-channel effect (Vth roll off) without increasing local variability unlike halo for bulk, low-leakage SRAM operation was demonstrated with adaptive-body-bias (ABB) scheme.

13.2 - 3:50 p.m.
Efficiency of Mechanical Stressors in Planar FDSOI n and p MOSFETs Down to 14nm Gate Length, S. Morvan, F. Andrieu, M. Cassé, O. Weber, N. Xu, P. Perreau, J.-M. Hartmann, J.-C. Barbé, J. Mazurier, P. Nguyen*, C. Fenouillet-Bérangee, C. Tabone, L. Tosti, L. Brévard, A. Toffoli, F. Allain, D. Lafond, B.-Y. Nguyen*, G. Ghibaudo^, F. Boeuf**, O. Faynot, T. Poiroux, CEA, LETI, MINATEC, *SOITEC, **STMicroelectronics, ^IMEP-LAHC/MINATEC

We fabricated highly stressed Fully Depleted Silicon-On-Insulator (FDSOI) n and pMOSFETs reaching ION,n/ION,p=1148/1014µA/µm drive current at IOFF,n/IOFF,p=55/16nA/µm leakage current (VDD=1V) with excellent VT-matching (AVT<1.5mV.µm). These short channel performances are well correlated and quantitatively explained by the effectiveness of strained SOI (sSOI), Contact-Etch-Stop-Layers (CESL) and SiGe raised sources and drains. sSOI improves ION,n up to 22% and degrades SiGe sources and drains efficiency for pMOSFETs. However, 0° (<110>) orientation remains the best configuration for high-stress pMOSFETs and provides the best trade-off for CMOS.

13.3 - 4:15 p.m.
Impact of Back Biasing on Carrier Transport in Ultra-Thin-Body and BOX (UTBB) Fully Depleted SOI MOSFETs, N. Xu, F. Andrieu*, B. Ho, B.-Y. Nguyen*, O. Weber*, C. Mazure*, O. Faynot*, T. Poiroux*, T.-J. King Liu, University of California, Berkeley, *CEA-LETI, Minatec, **SOITEC

A comprehensive study of the impact of back biasing on carrier transport behavior in Ultra-Thin Body and BOX (UTBB) Fully Depleted SOI (FD-SOI) MOSFETs and its implications for deeply scaled device performance is presented.

13.4 - 4:40 p.m.

Enhancement of Devices Performance of hybrid FDSOI/Bulk Technology by using UTBOX sSOI substrates, C. Fenouillet-Beranger, P. Perreau, O. Weber, I. Ben-Akkez*, A. Cros*, A. Bajolet*, S. Haendler*, P. Fonteneau*, P. Gouraud*, E. Richard*, F. Abbate*, D. Barge*, D. Pellissier-Tanon*, B. Dumont*, F. Andrieu, J. Passieux*, R. Bon*, V. Barral, D. Golanski*, D. Petit*, N. Planes*, O. Bonin**, W. Schwarzenbach**, T. Poiroux, O. Faynot, M. Haond*, F. Boeuf*, CEA-LETI, MINATEC, *STMicroelectronics, **SOITEC

For the first time, CMOS devices on UTBOX 25nm combined with strained SOI (sSOI) substrates have been demonstrated. A 20% Ion boost is highlighted with these substrates compared to the standard UTBB SOI ones. Performance up to 1530µA/µm @ Ioff=100nA/µm (Vd 1V) for a nominal Lg=30nm with a CET of 1.5nm for the NMOS has been achieved. The viability of this substrate has been demonstrated thanks to our hybrid process, through threshold voltage modulation and leakage current reduction, with back biasing for short devices. In addition, cell current improvement of 23% in 0.12µm2 bitcell is noticed for sSOI at the same stand-by current vs the standard UTBB SOI. Finally, the functionality of hybrid ESD device underneath the BOX is demonstrated.

13.5 - 5:05 p.m.

Strain Engineered Extremely Thin SOI (ETSOI) for High-Performance CMOS, A. Khakifirooz, K. Cheng, T. Nagumo*, N. Loubet**, T. Adam, A. Reznicek, J. Kuss, D. Shahrjerdi, R. Sreenivasan, S. Ponoth, H. He, P. Kulkarni, Q. Liu**, P. Hashemi[#], P. Khare**, S. Luning^, S. Mehta, J. Gimbert**, Y. Zhu[#], Z. Zhu[##], J. Li, A. Madan[##], T. Levin, F. Monsieur**, T. Yamamoto*, S. Naczas, S. Schmitz, S. Holmes, C. Aulnette^, N. Daval^, W. Schwarzenbach^, B-Y. Nguyen^, V. Parachuri, M. Khare, G. Shahidi[#], B. Doris, IBM Research, *Renesas, **STMicroelectronics, ^GLOBALFOUNDRIES, ^^SOITEC, [#]IBM TJ Watson Research Center, [##]IBM SRDC

High-performance strain-engineered ETSOI devices are reported. Three methods to boost the performance, namely contact strain, strained SOI (SSDOI) for NFET, and SiGe-on-insulator (SGOI) for PFET are examined. Significant performance boost is demonstrated with competitive drive currents of 1.65mA/µm and 1.25mA/µm and effective currents of 0.95mA/µm and 0.70mA/µm at Ioff =100nA/µm and VDD of 1V, for NFET and PFET, respectively.

Session 14 – TAPA 3

Novel Passive and Active BEOL Technologies

Wednesday, June 13, 3:25 p.m.
Chairs: R. Klein, AMD
H. Morimura, NTT Microsystem Integration Lab

14.1 - 3:25 p.m.

A Novel Chemically, Thermally and Electrically Robust Cu Interconnect Structure with an Organic Non-porous Ultralow-k Dielectric Fluorocarbon (k=2.2), X. Gu, A. Teramoto, R. Kuroda, Y. Tomita, T. Nemoto, S.-i. Kuroki, S. Sugawa, T. Ohmi, Tohoku University

A novel chemically, thermally and electrically robust Cu damascene interconnects with an organic non-porous ultralow-k (ULK) dielectric fluorocarbon (k=2.2), deposited by an advanced microwave excited plasma enhanced CVD, is demonstrated. A practical nitrogen plasma treatment (NPT) was employed to minimize chemically damage introduction to fluorocarbon in post-etching cleaning and CMP processes. Also, a new structure with a delamination-protective-liner (DPL), instead of barrier-metal, between Cu and fluorocarbon is introduced to avoid thermally induced electrical degradation and to reduce the interconnect delay significantly (by >30% in 32 nm-node). Non-porous ULK fluorocarbon with NPT and DPL technologies is a promising candidate for high performance Cu interconnects.

14.2 - 3:50 p.m.

Graphene Interconnect Lifetime Under High Current Stress, X. Chen, D. Seo*, S. Seo**, H. Chung*, H.-S.P. Wong, Stanford University, *Samsung Advanced Institute of Technology, **Sejong University

Lifetime of multi-layer graphene interconnects under constant current stress is studied for the first time. Under a stress current density of 20MA/cm2 at 250°C exposed to air, Mean-Time-To-Fail (MTTF) of uncapped CVD graphene wire is about 6 hours. It is shown that lifetime is mainly limited by defect formation due to graphene oxidation.

14.3 - 4:15 p.m.
Operation of Functional Circuit Elements using BEOL-Transistor with InGaZnO Channel for On-chip High/Low Voltage Bridging I/Os and High-Current Switches, K. Kaneko, H. Sunamura, M. Narihiro, S. Saito, N. Furutake, M. Hane, Y. Hayashi, Renesas Electronics Corporation

Functional circuit elements based on novel BEOL-transistors with a wide-band-gap oxide semiconductor InGaZnO (IGZO) film are integrated onto LSI Cu-interconnects, and their operations are demonstrated. High-current comb-type transistors show excellent Ion/Ioff ratio (>108) and high-Vd operation with linear area dependence, realizing area-saving compact high-current BEOL switches. Successful operation of voltage-controlled inverter switches with high-Vd enables on-chip bridging I/Os between high/low voltage on conventional Si system LSIs. Setting the gate-to-drain offset design to just 0.1□m realizes +20V enhancement of the breakdown voltage to ~60V with excellent safety operation at around Vd=50V due to the wide-band-gap characteristics.

14.4 - 4:40 p.m.
High Performance Bilayer Oxide Transistor for Gate Driver Circuitry Implemented on Power Electronic Devices, S. Jeon, H. Kim, H. Choi, I. Song, S.-E. Ahn, C.J. Kim, J. Shin, U.-I. Chung, I. Yoo, K. Kim, Samsung Electronics Co.

The integration of electronically active oxide transistors onto silicon circuits represents an innovative approach to improving the performance of devices. In this paper, we present high performance oxide transistors for use as gate drive circuitry integrated on top of a power electronic device, providing a novel power system. With this approach, we aim to reduce the form factor, cost, weight and noise of power management integrated circuitry (PMIC). Specifically, as a core device component in gate driver, oxide transistor exhibits remarkable performance such as, high mobility (23~47cm2/Vs) and high breakdown voltages of 60~340V despite low process temperatures (<300°C). In addition, we demonstrate the dynamic behavior of the inverter and the latch produced by oxide transistor and thus a complete and functioning gate drive circuitry can be implemented on top of PMIC as depicted in this report. We also discuss carrier transport mechanism of bi-layer oxide transistor through the assessment of low frequency noise property, which gives a further insight in the underlying physics of oxide transistor.

14.5 - 5:05 p.m.
Sub-fM DNA Sensitivity by Self-Aligned Maskless Thin-Film Transistor-Based SoC Bioelectronics, M.-C. Chen, C.-H. Lin, C.-Y. Lin, F.-K. Hsueh, W.-H. Huang, Y.-C. Lien, H.-C. Chen, H.-T. Hsueh*, C.-W. Huang*, C.-T. Lin*, Y.-C. Liu**, T.-H. Lee**, M.-Y. Hua, J.-T. Qiu, M.-C. Liu, Y.-J. Lee, J.-M. Shieh, C. Ho, C. Hu^, F.-L. Yang, National Nano Device Laboratories, *National Taiwan University, **Chang Gung University, University of California, Berkeley

This is the first study to successfully achieve record DNA sensitivity (sub-fM) by self-aligned, maskless, dual-channel, and metal-gate-based thin-film transistor nano-wire FET. Both novel device architecture (dual-channel) and optimization of integration processes (microcrystalline silicon and self-aligned sidewall sub-50 nm critical dimension) of nano-wire FET enhance the sensitivity to biological entities substantially. Meanwhile, the proposed device is accomplished with an embedded VLSI CMOS circuit. It can thus offer high application potential to pH, protein, and DNA probing in SoC-based portable bioelectronics.

Session 15 – TAPA 2
CMOS Platform

Thursday, June 14, 8:05 a.m.
Chairs: W. Maszara, Globalfoundries

S. Inaba, Toshiba Corp.

15.1 - 8:05 a.m.

High Performance Bulk Planar 20nm CMOS Technology for Low Power Mobile Applications, H. Shang, S. Jain, E. Josse*, E. Alptekin, M.H. Nam**, S.W. Kim^, K.H. Cho^, I. Kim^, Y. Liu**, X. Yang**, X. Wu**, J. Ciavatti**, N.S. Kim**, R. Vega, L. Kang**, H.V. Meer**, S. Samavedam**, M. Celik*, S. Soss**, H. Utomo, R. Ramachandran, W. Lai, V. Sardesai, C. Tran, J.Y. Kim^, Y.H. Park^, W.L. Tan**, T. Shimizu^^, R. Joy**, J. Strane, K. Tabakman, F. Lalanne*, P. Montanini*, K. Babich**, J.B. Kim^, L. Economikos, W. Cote, C. Reddy**, M. Belyansky, R. Arndt, U. Kwon, K. Wong, D. Koli**, D. Leveakis, J.W. Lee^, J. Muncy, S. Krishnan, D. Schepis, X. Chen, B.D. Kim^, C. Tian, B.P. Linder, E. Cartier, V. Narayanan, G. Northrop, O. Menut*, J. Meiring, A. Tomas, M. Aminpur, S.H. Park^, K.Y. Weybright, R. Mann**, A. Mittal**, M. Eller#, S. Lian^, R. Divakaruni, S. Bukofsky, J.D. Kim^, J. Sudijono**, W. Neumueller#, F. Matsuoka^^, R. Sampson*, IBM Microelectronics, *STMicroelectronics, **GLOBALFOUNDRIES, ^Samsung Electronics, ^^Toshiba Corporation, #IMC GmbH

In this paper, we present a high performance planar 20nm CMOS bulk technology for low power mobile (LPM) computing applications featuring an advanced high-k metal gate (HKMG) process, strain engineering, 64nm metal pitch & ULK dielectrics. Compared with 28nm low power technology, it offers 0.55X density scaling and enables significant frequency improvement at lower standby power. Device drive current up to 2X 28nm at equivalent leakage is achieved through co-optimization of HKMG process and strain engineering. A fully functional, high-density (0.081um2 bit-cell) SRAM is reported with a corresponding Static Noise Margin (SNM) of 160mV at 0.9V. An advanced patterning and metallization scheme based on ULK dielectrics enables high density wiring with competitive R-C.

15.2 - 8:30 a.m.

A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors, C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyun, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roester, J. Sanford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, G. Weber, P. Yashar, K. Zawadzki, K. Mistry, Intel Corp.

A 22nm generation logic technology is described incorporating fully-depleted tri-gate transistors for the first time. These transistors feature a 3rd-generation high-k + metal-gate technology and a 5th generation of channel strain techniques resulting in the highest drive currents yet reported for NMOS and PMOS. The use of tri-gate transistors provides steep subthreshold slopes (~70mV/dec) and very low DIBL (~50mV/V). Self-aligned contacts are implemented to eliminate restrictive contact to gate registration requirements. Interconnects feature 9 metal layers with ultra-low-k dielectrics throughout the interconnect stack. High density MIM capacitors using a hafnium based high-k dielectric are provided. The technology is in high volume manufacturing.

15.3 - 8:55 a.m.

28nm FDSOI Technology Platform for High-Speed Low-Voltage Digital Applications, N. Planes, O.Weber*, V. Barral*, S. Haendler, D. Noblet, D. Croain, M. Bocat, P.-O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau*, D. Petit, D. Golanski, C. Fenouillet-Beranger*, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M.-A. Jaud*, O. Rozeau*, O. Saxod, F. Wacquant, F. Monsier, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, M. Haond, STMicroelectronics, *CEA-LETI, MINATEC

For the first time, a full platform using FDSOI technology is presented. This work demonstrates 32% and 84% speed boost at 1.0V and 0.6V respectively, without adding process complexity compared to standard bulk technology. We show how memory access time can be significantly reduced thanks to high Iread, by keeping competitive leakage values. Yield of ~14Mb SRAM cells is demonstrated, allowing to measure for the first time Vmin of SRAM arrays.

15.4 - 9:20 a.m.

Advanced Modeling and Optimization of High Performance 32nm HKMG SOI CMOS for RF/Analog SoC Applications, S. Lee, J. Johnson, B. Greene, A. Chou, K. Zhao, M. Chowdhury, J. Sim, A. Kumar, D. Kim, A. Sutton, S.H. Ku, Y. Liang, Y. Wang, D. Slisher, K. Duncan, P. Hyde, R. Thoma, J. Deng, Y. Deng, R. Rupani, R. Williams, L. Wagner, C. Wermer, H. Li, B.

Johnson, D. Daley, J.O. Plouchart, S. Narasimha, C. Putnam, E. Maciejewski, W. Henson, S. Springer, IBM Semiconductor Research and Development Center

We demonstrate advanced modeling and optimization of 32nm high-K metal gate (HKMG) SOI CMOS technology for high-speed digital and RF/analog system-on-chip applications. To enable high-performance RF/analog circuit design, we present challenging device modeling features and their enhancements. At nominal Lpoly, floating-body NFET and PFET demonstrate peak fT of 300GHz and fMAX of higher than 350GHz with excellent model-to-hardware accuracy. For precision analog circuit design, body-contacted (BC) FETs and various passives are offered, and their performance and modeling accuracy are co-optimized to push the technology limit and achieve state-of-the-art circuits, e.g., 28Gb/s serial link transceiver and LC-tank VCO operating at higher than 100GHz.

Session 16 – TAPA 3

Noise Phenomena

Thursday, June 14, 8:05 a.m.
Chairs: C. Mazure, SOITEC Group
S.S. Chung, Nat'l Chiao Tung Univ.

16.1 - 8:05 a.m.

Voltage and Temperature Dependence of Random Telegraph Noise in Highly Scaled HKMG ETSOI nFETs and its Impact on Logic Delay Uncertainty, H. Miki, M. Yamaoka, D.J. Frank*, K. Cheng*, D.-G. Park*, E. Leobandung*, K.Torii**, Hitachi America, Ltd., IBM Corp, **Hitachi Ltd.

This paper analyzes the extensive variability of random telegraph noise (RTN) responses to gate voltage and temperature in undoped nanoscale nFETs. Using comprehensive RTN measurements to extract the response parameters of >600 traps, we show that the RTN can induce delay uncertainty in dense low power (i.e., narrow devices and low VDD) 14-nm technology that may exceed 50% of the nominal delay.

16.2 - 8:30 a.m.

New Insights into AC RTN in Scaled High-k/Metal-Gate MOSFETs Under Digital Circuit Operations, J. Zou, R. Wang, N. Gong, R. Huang, X. Xu, J. Ou, C. Liu, J. Wang*, J. Liu*, J. Wu*, S. Yu*, P. Ren, H. Wu*, S.-W. Lee*, Y. Wang, Peking University, *SMIC

Since devices actually operate under AC signals in digital circuits, it is more informative to study random telegraph noise (RTN) at dynamic AC biases than at constant DC voltages. We found that the AC RTN statistics largely deviates from traditional DC RTN, in terms of different distribution functions and the strong dependence on AC signal frequency, which directly impacts on the accurate prediction of circuit stability and variability. The AC RTN characteristics in high-k/metal-gate FETs are different from that in SiON FETs, and both of which cannot be described by classical RTN theory. A physical model based on quantum mechanics is proposed, which successfully explains the new observations of AC RTN. It is also demonstrated that, if using DC RTN statistics instead of AC RTN, a large error on the read failure probability in ultra-scaled SRAM cells will occur.

16.3 - 8:55 a.m.

Comprehensive Investigations on Neutral and Attractive Traps in Random Telegraph Signal Noise Phenomena using (100)- and (110)-Orientated CMOSFETs, J. Chen, I. Hirano, K. Tatsumura, Y. Mitani, Toshiba Corporation

Neutral traps and attractive traps in random telegraph Noise(RTN) on both (100)- and (110)-orientated CMOSFETs are well distinguished and systematically studied for the first time, including both electron and hole traps. It is found that neutral traps energy distributions are higher than attractive traps and, most importantly, neutral traps caused much larger threshold voltage shifts (ΔV_{th_RTN}) than attractive traps do, especially in (110)-nMOSFETs. Furthermore, based on obtained ΔV_{th_RTN} in CMOSFETs of various orientation surfaces, 3D FinFET structure optimizations are discussed in view of ΔV_{th_RTN} suppression.

16.4 - 9:20 a.m.
Continuous Characterization of MOSFET From Low-Frequency Noise to Thermal Noise Using a Novel Measurement System up to 100 MHz, K. Ohmori, R. Hasunuma, W. Feng, K. Yamada, University of Tsukuba

We have developed a novel system for characterizing higher-frequency noise properties of MOSFETs under DC-biases up to 100 MHz. A low-noise amplifier (LNA) was mounted on a unique micro probe-card so that the signal from DUT (on a wafer) is captured with lesser losses. Using this new approach, we have successfully demonstrated the transition of low-frequency (LF) noise to high-frequency (HF) noise, such as thermal noise. In addition, the change in the factors of noise results in lowing the standard variation of noise in a HF region, where intrinsic phenomena derived from the channel conductance play a key roll.

Session 17 – TAPA 2
Technology / Circuits Joint Focus Session – Design in Scaled Technologies

Thursday, June 14, 10:00 a.m.
Chairs: J. Cheek, Freescale
R. Takemura, Hitachi, Ltd.

17.1 – 10:00 a.m.
Design Enablement at 14nm: The Challenge of Being Early, Accurate, and Complete (Invited), M.E. Mason, Texas Instruments

Progress evidenced by Moore's Law has driven increased performance at decreased cost per function. Often, the price of this progress is balanced against complexity and time-to-market (both directly impacting cost). Design enablement teams must mitigate these cost factors by delivering accurate process design kits (PDKs) that predict both process and device performance at production on a schedule that supports time-to-market goals. Here, we examine some key technology issues affecting the critical relationship between process, device, design and products.

17.2 – 10:25 a.m.
Designing in Scaled Technologies: 32nm and Beyond (Invited), S. Kosonocky, T. Burd, K. Kasprak, R. Schultz, R. Stephay, AMD

VLSI technology scaling in the 32-nm node and beyond has presented designers with increasing challenges to obtain performance gains, power and area reductions each successive generation. Maximum voltage limits, decreasing interconnect performance and reliability, and device changes have forced designers to rethink system and circuit design for enhanced system performance and improved user experience. This paper will review some of the challenges and potential solutions to designing in advanced nodes including bias temperature instabilities (BTI), time-dependent dielectric breakdown (TDDB), metal pitch scaling limitations, electro-migration, and challenges designing with next generation CMOS devices.

17.3 – 10:50 a.m.
The Optimum Device Parameters for High RF and Analog/MS Performance in Planar MOSFET and FinFET (Invited) T. Ohguro, Y. Higashi, K. Okano, S. Inaba, Y. Toyoshima, Toshiba

For analog and RF designer, higher fT, fmax and low flicker noise are attractive to realize the high performance circuit. The scaled planar MOSFET has lead to the higher operation frequency application. Recently, un-doped double gate MOSFETs, such as FinFET are promising candidates for scaling CMOS into the sub-32nm node and below because of its good cut-off characteristics and better scalability due to double gate mode operation. However, reported figure of merit of FinFET are lower than planar MOSFET [3, 4]. In this paper, we discuss device parameter to obtain high RF performance for planar MOSFET and FinFET. Additionally, structural merits of FinFET relative to flicker noise are discussed.

17.4 – 11:15 a.m.
Dynamic Intrinsic Chip ID Using 32nm High-K/Metal Gate SOI Embedded DRAM, D. Fainstein, S. Rosenblatt, A. Cestero, N. Robson, T. Kirihata, S.S. Iyer, IBM Systems and Technology Group

A random intrinsic chip ID method generates a pair of 4Kb binary strings using retention fails in 32nm SOI embedded DRAM. Hardware results show ID overlap distance mean=0.58 and σ=0.76 and demonstrate 100% authentication for 346 chips. The analytical model predicts > 99.999% unique IDs for 10^6 parts.

17.5 – 11:40 a.m.
A Fully-Digital Phase-Locked Low Dropout Regulator in 32nm CMOS, A. Raychowdhury, D. Somasekhar, J. Tschanze, V. De, Intel Corp.

A fully-digital phase-locked low dropout regulator (LDO) has been designed in 32nm CMOS for fine-grained power delivery to multi-Vcc digital circuits. Measurements across a wide range of input voltages and currents exhibit that the LDO offers excellent load regulation and efficiency close to 97% of ideal efficiency at nominal load current conditions (ILOAD=3mA).

Session 18 – TAPA 3
RRAM II

Thursday, June 14, 10:00 a.m.
Chairs: G. Jurczak, IMEC
Y. Nakao, Rohm Co., Ltd.

18.1 - 10:00 a.m.
Integration of 4F2 Selector-less Crossbar Array 2Mb ReRAM Based on Transition Metal Oxides for High Density Memory Applications, H.D. Lee, S.G. Kim, K. Cho, H. Hwang, H. Choi, J. Lee, S.H. Lee, H.J. Lee, J. Suh, S.-O. Chung, Y.S. Kim, K.S. Kim, W.S. Nam, J.T. Cheong, J.T. Kim, S. Chae, E.-R. Hwang, S.N. Park, Y.S. Sohn, C.G. Lee, H.S. Shin, K.J. Lee, K. Hong, H.G. Jeong, K.M. Rho, Y.K. Kim, S. Chung, J. Nickel, J.J. Yang, H.S. Cho, F. Perner, R.S. Williams, J.H. Lee, S.K. Park, S.-J. Hong, Hynix Semiconductor Inc.

4F2 selector-less crossbar array 2Mb ReRAM test chip with 54nm technology has been successfully integrated for high cell efficiency and high density memory applications by implementing parts of decoders to row/column lines directly under the cell area. Read/write specifications for memory operation in a chip are presented by minimizing sneak current through unselected cells. The characteristics of memory cell (nonlinearity, Kw >8, Iop <10uA, Vop <3V), TiOx/Ta2O5, are modified for its working in a chip by adopting appropriate materials for a resistor stack and spacer. Write condition in a chip makes a critical impact on read margin and read/write operation in a chip has been verified.

18.2 - 10:25 a.m.
Multi-Layer Sidewall WO_X Resistive Memory Suitable for 3D ReRAM, W.C. Chien, F.M. Lee, Y.Y. Lin, M.H. Lee, S.H. Chen, C.C. Hsieh, E.K. Lai, H.H. Hui, Y.K. Huang, C.C. Yu, C.F. Chen, H.L. Lung, K.Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd.

An easy to fabricate, low-cost, multi-layer sidewall WOX ReRAM device is proposed for 3D ReRAM application. A 2-layer (10nm x 100nm) device is fabricated and characterized for the first time. The WOX is grown by conventional RTO process but a special semi-permeable TiN (SP-TiN) is developed to achieve the necessary extrusion-free structure for 3D ReRAM. The multi-layer sidewall WOX ReRAM devices show characteristics similar to planar devices, but the reasons for layer-to-layer variation and some performance degradation still need to be understood.

18.3 - 10:50 a.m.
Ultrathin (<10nm) Nb_2O_5/NbO_2 Hybrid Memory with Both Memory and Selector Characteristics for High Density 3D Vertically Stackable RRAM Applications, S. Kim, X. Liu, J. Park, S. Jung, W. Lee, J. Woo, J. Shin, G. Choi, C. Cho, S. Park, D.

Lee, E.-j. Cha, B.-H. Lee, H.D. Lee, S.G. Kim, S. Jung, H. Hwang, Gwangju Institute of Science and Technology, *Hynix Semiconductor Inc.

We report, for the first time, the novel concept of ultrathin (~10nm) W/NbOx/Pt device with both threshold switching (TS) and memory switching (MS) characteristics. Excellent TS characteristics of NbO2, such as high temperature stability (~160oC), fast switching speed (~22ns), good switching uniformity, and extreme scalability of device area (ϕ~10nm)/thickness (~10nm) were obtained. By oxidizing NbO2, we can form ultrathin Nb2O5/NbO2 stack layer for hybrid memory devices with both TS and MS. Without additional selector device, 1Kb cross-point hybrid memory device without SET/RESET disturbance up to 106 cycles was demonstrated.

18.4 - 11:15 a.m.
Process-Improved RRAM Cell Performance and Reliability and Paving the Way for Manufacturability and Scalability for High Density Memory Application, G.S. Kar, A. Fantini, Y.Y. Chen, V. Paraschiv, B. Govorean, H. Hody, N. Jossart, H. Tielens, S. Brus, O. Richard, T. Vandeweyer, D. Wouters, L. Altimime, M. Jurczak, imec

Here for the first time we discuss RRAM cell performance and reliability through process improvement. Excellent post-cycling (1E6) retention and post-bake retention and endurance have been achieved for the optimized process conditions. The optimized RRAM cells show potential for manufacturability and scalability for high density memory application.

18.5 - 11:40 a.m.
Ultralow Sub-500nA Operating Current High-Performance TiN\\$Al_2O_3$\\$HfO_2$\Hf\TiN Bipolar RRAM Achieved Through Understanding-Based Stack-Engineering, L. Goux, A. Fantini, G. Kar, Y.-Y. Chen, N. Jossart, R. Degraeve, S. Clima, B. Govoreanu, G. Lorenzo, G. Pourtois, D.J. Wouters, J.A. Kittl, L. Altimime, M. Jurczak, imec

We demonstrate sub-500nA switching and tunable set voltage by inserting thin Al2O3 layer in TiN\HfO2\Hf\TiN RRAM cell. Stack engineering clearly led to novel insights into the switching phenomenology: (i) O-scavenging is key in the forming process and stack-asymmetry management; (ii) dielectric-stack thinning allows lower forming current; (iii) 'natural' (asymmetry-induced) reset switching takes place close to the TiN anode; (iv) reset resistance is limited by material-barrier properties at TiN interface

Session 19 – TAPA 2
High Mobility – Ge Devices

Thursday, June 14, 1:30 p.m.
Chairs: T. Ernst, CEA-LETI, MINATEC
T. Tanaka, Fujitsu Semiconductor

19.1 - 1:30pm
High Mobility Ge pMOSFETs with 0.7 nm Ultrathin EOT using HfO_2/Al_2O_3/GeO_x/Ge Gate Stacks Fabricated by Plasma Post Oxidation, R. Zhang, P.-C. Huang, N. Taoka, M. Takenaka, S. Takagi, University of Tokyo

HfO2/Al2O3/GeOx/Ge gate stacks were fabricated by applying the plasma post oxidation to HfO2/Al2O3/Ge structures. These Ge gate stack are shown to simultaneously realize both ultrathin EOT of ~0.7 nm and low Dit of 1011 cm-2eV-1 order. The superior operation of (100) Ge pMOSFETs with these gate stacks has been demonstrated with record high hole mobility of 596 cm2/Vs under ~0.8 nm EOT among the Ge pMOSFETs reported so far.

19.2 - 1:55pm
85nm-Wide 1.5mA/µm-I_{ON} IFQW SiGe-pFET: Raised vs Embedded $Si_{0.75}Ge_{0.25}$S/D Benchmarking and In-Depth Hole Transport Study, J. Mitard, L. Witters, G. Eneman, G. Hellings, L. Pantisano, A. Hikavyy, R. Loo, P. Eyben, N. Horiguchi, A. Thean, Imec

Beside the VTH-tunability, we found that a raised SiGe S/D module offers higher LG-scalability than an embedded SiGe S/D in SiGe-IFQW pFETs. An in-depth transport study of record performing 1.5mA/µm-ION 85x35nm2 strained-SiGe Implant Free Quantum Well (IFQW) pFETs reveals that mobility improvement is still the key performance booster whereas LG-scaling has finally a limited impact.

19.3 - 2:20pm
High-Mobility and Low-parasitic Resistance Characteristics in Strained Ge Nanowire pMOSFETs with Metal Source/Drain Structure Formed by Doping-free Processes, K. Ikeda, M. Ono, D. Kosemura*, K. Usuda, M. Oda, Y. Kamimuta, T. Irisawa, Y. Moriyama, A. Ogura, T. Tezuka, AIST, *Meiji University

Metal source/drain (S/D) Ge nanowire MOSFETs with a compressive strain as high as 3.8% were fabricated by the 2-step Ge-condensation technique without intentional doping for the S/D. Record high inversion hole mobility (855 cm2/Vs @ Ns = 5e12cm-2) and saturation drain current 731uA/um at Vd=-1V were achieved among Ge nanowire pFETs ever reported. It is found that the extremely low contact resistivity ~ 4e-8 ohm-cm2 for the Schottky contact contributes to the high saturation current as well as the high mobility.

19.4 - 2:45 p.m.
Segmented-Channel $Si_{1-x}Ge_x$/Si pMOSFET for Improved I_{ON} and Reduced Variability, B. Ho, N. Xu, B. Wood*, V. Tran*, S. Chopra*, Y. Kim*, B.-Y. Nguyen**, O. Bonnin**, C. Mazure**, S. Kuppurao*, C.-P. Chang*, T.-J. King Liu, University of California, Berkeley, *Applied Materials, **SOITEC

Segmented-channel Si(1-x)Ge(x)/Si pMOSFETs are fabricated using a conventional process, starting with a corrugated Si(1-x)Ge(x)/Si substrate. As compared with control devices fabricated using the same process but starting with a non-corrugated Si(1-x)Ge(x)/Si substrate, the segmented-channel MOSFETs show better layout efficiency (30% higher ION for IOFF=10 nA per µm layout width) due to enhanced hole mobility, and dramatically reduced dependence of performance on layout width due to the geometrical regularity of the channel region.

Session 20 - TAPA 3
3D Integration Technology

Thursday, June 14, 1:30 p.m.
Chairs: A. Antonelli, Novellus Systems, Inc.
T. Tanaka, Tohoku Univ.

20.1 - 1:30 p.m.
Ultrafast Parallel Reconfiguration of 3D-Stacked Reconfigurable Spin Logic Chip with On-chip SPRAM (SPin-transfer torque RAM), T. Tanaka, H. Kino, R. Nakazawa, K. Kiyoyama*, H. Ohno, M. Koyanagi, Tohoku University, *Nagasaki Institute of Applied Science

We have developed novel 3D-stacked reconfigurable spin logic chip having ultrafast on-chip SPRAM to overcome drawbacks of conventional reconfigurable LSIs. Two reconfigurable spin logic chips were carefully designed and successfully stacked using 3D integration technology. From the SPRAM cell evaluation, the fastest write speed of 5 ns was obtained in the circuits. To realize higher performance reconfigurable LSIs, parallel reconfiguration was fully demonstrated for the stacked reconfigurable spin logic chips for the first time. Both ultrafast on-chip SPRAM and 3D-stacked structure will open a new era of reconfigurable LSIs.

20.2 - 1:55 p.m.
Development of Ultra-Thin Chip-on-Wafer Process Using Bumpless Interconnects for Three-Dimensional Memory/Logic Applications, N. Maeda, H.Kitada, K. Fujimoto**, Y. Kim, S.Kodama*, S.Yoshimi**, M. Akazawa**, Y. Mizushima^, T. Ohba, University of Tokyo, *DISCO Corporation, **Dai Nippon Printing, ^Fujitsu Laboratory Ltd.

Chip-on-Wafer (COW) stacking structure using stack-first and bumpless interconnects was successfully fabricated for the first time. Chips were arrayed and bonded onto the wafer by back-to-face and gap filling between chips were carried out

using organic material without void formation. Chips on the wafer were thinned down to 5 μm. Via-holes were formed at off-chip area (outside the chip). Copper redistribution line was formed using the via-first Damascene method. Lower leakage current as low as back ground was found between pads. No failure and an approximate 100% yield were achieved in the vertical wiring for multi-chips COW stacking.

20.3 - 2:20 p.m.
High-Aspect Ratio Through Silicon Via (TSV) Technology, H.-P. Chang, H.-Y. Chen, P.-C. Kuo, A. Chien, E. Liao, T.-C. Lin, J. Wei, Y.-C. Lin, Y.-H. Chen, K.-F. Yang, H.-A. Teng, J. Tsai, Y.C. Tseng, S.Y. Chen, C.-C. Hsieh, M.F. CHEN, Y.-H. Liou, T.-J. Wu, S. Y. Hou, W.-C. Chiou, S.-P. Jeng, C.-H.Yu, Taiwan Semiconductor Manufacturing Company, Ltd.

The density of through-silicon-via (TSV) on CMOS chip is limited by TSVdimension and keep-out zone (KOZ). A high aspect ratio Cu TSV process, 2 mmx 30 mm, is demonstrated on 28nm CMOS baseline with good electricalperformance and low cost. By implementing 2 mm x 30 mm TSV, the Si stressin the vicinity of TSV caused by thermal expansion is able to be relieved.It is, therefore, shown that the relaxation of TSV stress is correlatedwith minimized keep-out zone (KOZ). The achievement of excellentperformance of 3D-IC yield and high aspect ratio TSV embedded devicecharacteristics are key milestones in the promising manufacturability of3D-IC by silicon foundry technology.

20.4 - 2:45 p.m.
Demonstration of Inter-chip Data Transmission in a Three-dimensional Stacked Chip Fabricated by Chip-level TSV Integration, K. Hozawa, F. Furuta, Y. Hanaoka, M. Aoki, K. Osada, K. Takeda, K.W. Lee*, T. Fukushima*, M. Koyanagi*, ASET, *Tohoku University

Successful 3D integration of a stacked chip fabricated by a “chip-level through-silicon-via (TSV)” process was confirmed by inter-chip data transmission. According to measurements of the electrical properties of the stacked chip, structural design of TSV contact wiring is very important for chip-level/via-last TSV integration. That is, the design influences TSV contact resistance, TSV coupling capacitance, and wiring capacitance of the surrounding Cu/low-k interconnections.

Session 21 – TAPA 2

Scaled III-V Transistors and Modeling

Thursday, June 14, 3:25 p.m.
Chairs: J. Kavalieros, Intel Corp.
B.H. Lee, Gwangju Institute of Sci. and Tech.

21.1 - 3:25 p.m.
Sub-60 nm Deeply-Scaled Channel Length Extremely-thin Body In_xGa_{1-x}As-On-Insulator MOSFETs on a Si with Ni-InGaAs Metal S/D and MOS Interface Buffer Engineering, S. Kim, M. Yokoyama, N. Taoka, R. Nakane, T. Yasuda*, O. Ichikawa**, N. Fukuhara**, M. Hata**, M. Takenaka, S. Takagi, University of Tokyo, *National Institute of Advanced Industrial Science and Technology, **Sumitomo Chemical Co., Ltd.

We report the first demonstration of sub-60 nm deeply-scaled InGaAs- and InAs-on-insulator MOSFETs on Si substrates with MOS interface buffer engineering and Ni-InGaAs metal source/drain (S/D). The devices provide 400 % I_{on} enhancement, when comparing to that of an In_{0.53}Ga_{0.47}As control device with the same drain-induced-barrier-lowering (DIBL) of 100 mV/V, which is attributable to the mobility enhancement and the S/D parasitic resistance (R_{SD}) reduction. In addition, InAs-OI MOSFETs with the MOS interface buffer show excellent electrostatic characteristics. A MOSFET with channel length (L_{ch}) of 55 nm shows small DIBL of 84 mV/V and subthreshold slope (S.S.) of 105 mV/dec, both of which do not significantly degrade with a decrease of L_{ch}, because of the extremely-thin channel thickness.

21.2 - 3:50 p.m.

InAs Quantum-Well MOSFET (L_g = 100 nm) with Record High g_m, f_T and f_{max}, T.-W. Kim, R. Hill, C.D. Young, D. Veksler, L. Morassi*, S. Oktybrshky**, J. Oh, C.Y. Kang, D.-H. Kim^, J.A. Del Alamo^^, C. Hobbs, P. Kirsch, R. Jammy, SEMATECH, *University of Modena and Emilia, **CNSE, ^Teledyne, ^^Massachusetts Institute of Technology

This paper reports InAs quantum-well (QW) MOSFETs with record transconductance (gm,max = 1.73 mS/µm) and high-frequency performance (fT = 245 GHz and fmax = 355 GHz) at Lg = 100 nm. This record performance is achieved by using a low Dit composite Al2O3/InP gate stack, optimized layer design and a high mobility InAs channel.

21.3 - 4:15 p.m.
Antimonide NMOSFET with Source Side Injection Velocity of 2.7×10^7 cm/s for Low Power High Performance Logic Applications, A. Ali, H. Madan, M. Barth, M. Hollander, B. Boos*, B. Bennett*, S. Datta, The Pennsylvania State University, *Naval Research LAb

Antimonide (Sb) quantum well (QW) MOSFETs are demonstrated with integrated high-k dielectric (1nmAl2O3-10nm HfO2). The long channel Sb NMOS exhibits effective electron mobility of 6,000 cm2/Vs at high field (2 x 1012 /cm2 of charge density (Ns)), which is the highest reported value for any III-V MOSFET. The short channel Sb NMOSFET (LG = 150nm) exhibits a cut-off frequency (fT) of 120GHz, fT - LG product of 18GHz.µm and source side injection velocity (veff) of 2.7x107 cm/s, at drain bias (VDS) of 0.75V and gate overdrive of 0.6V. The measured fT and fT x LG are 2 x higher, and veff is 4x higher than Si NMOS (1.0-1.2V VDD) at similar LG, and are the highest for any III-V MOSFET.

21.4 - 4:40 p.m.
Understanding the Feasibility of Scaled III-V TFET for Logic By Bridging Atomistic Simulations and Experimental Results, U.E. Avci, S. Hasan, D.E. Nikonov, R. Rios, K. Kuhn, I.A. Young, Intel Corporation

A detailed comparison between III-V TFET's experimental characteristics and atomistic quantum mechanical predictions is reported to study the validity of the performance improvement predictions of a scaled TFET. Simulations did not employ any fitting parameters to match the experimental data, but instead used material and geometry parameters as the only inputs. The results show that the experimental and simulation characteristics are in reasonable agreement, suggesting that the experimental devices are without significant unknown effects or defects, and the atomistic simulations have good predictability. The differences between scaled TFET predictions and large experimental TFET devices are shown to be due to the geometry, meaning that improved electrostatics with thin body and double-gate is required for TFET scaling. Results demonstrate that the III-V TFET is a realistic candidate for future low-voltage logic applications.

21.5 - 5:05 p.m.
InGaSb: Single Channel Solution for Realizing III-V CMOS, Z. Yuan, A. Nainani*, A. Kumar, X. Guan, B. R. Bennett**, J.B. Boos**, M.G. Ancona**, K.C. Saraswat, Stanford University, *Applied Materials, **Naval Research Lab

There has been an upsurge of interest in the possibility of a low-power, high-performance CMOS based on III-V materials. For such a technology to be realized, advances are needed in a number of areas including: (a) comparable high performance from n- and p-channel devices for complementary logic; (b) reducing the impact of Dit; and (c) overcoming low density of states (DOS) of electrons which could limit the NMOS ION. In this study, methods are investigated that deliver improvements in these three areas. We chose to work on the 6.1-6.2Å lattice constant system with InGaSb as the channel material because of its advantages in terms of band engineering and high mobility/offsets for both electrons and holes. Despite its larger lattice constant, antimonide's are also found to be potentially more suitable for hetero-integration. We demonstrate electron/hole mobility > 4000/900cm2/Vs can be achieved in a single channel material. For the first time in III-V systems, both n- and p-channel transistors with one single channel material show comparable high on-current.

Session 22 – TAPA 3
Variability Characterization and Modeling

Thursday, June 14, 3:25 p.m.

Chairs: T. Skotnicki, STMicroelectronics
N. Sugii, Hitachi, Ltd.

22.1 - 3:25 p.m.

Threshold Voltage and DIBL Variability Modeling for SRAM and Analog MOSFETs, N. Damrongplasit, L. Zamudio*, S. Balasubramanian*, University of California, Berkeley, *GLOBALFOUNDRIES

A physically-based variability model is developed to explain threshold voltage (VT) and drain induced barrier lowering (DIBL) variations, and their correlations. Inputs to the model rely on forward (F) and reverse (R) data of measured transistor pair mismatch. Positionally asymmetric and symmetric random dopant fluctuation components of VT and DIBL variability are identified for SRAMs and analog devices from a 32nm HKMG technology and their correlations explained.

22.2 - 3:50 p.m.

The Understanding of the Trap Induced Variation in Bulk Tri-Gate Devices by a Novel Random Trap Profiling (RTP) Technique, H.M. Tsai, E.R. Hsieh*, S.S. Chung, C.H. Tsai, R.M. Huang*, C.T. Tsai*, C.W. Liang*, National Chiao Tung University, *United Microelectronics Corporation

Not only the popular random dopant fluctuation (RDF), but also the traps, caused by the HC stress or NBTI-stress, induce the Vth variations. To identify these traps, for the first time, a unique random trap profiling feasible for 3D device applications has been demonstrated on trigate devices. For such devices, the oxide traps are generated not only near the drain side but also on the sidewall, after hot carrier(HC) and NBTI stresses. More importantly, the Vth variation in pMOSFET under NBTI becomes much worse as a result of an additional surface roughness effect. This method provides us a valuable tool for the diagnosis of reliability in 3D devices (e.g., FinFET).

22.3 - 4:15 p.m.

Accurate Chip Leakage Prediction: Challenges and Solutions, X. Yu, J. Deng, S. Loo, K. Dezfulian, S. Lichtensteiger*, J. Bickford*, N. Habib*, P. Chang, A. Mocuta, K. Rim, IBM SRDC, *IBM System and Technology Group

A systematic method is proposed to address modeling challenges in accurate chip level leakage prediction, namely a precise total leakage width count method, a simple model to quantify leakage uplift caused by systematic across-chip variation, and a consistent model to capture 3-sigma leakage and leakage spread at fixed performance.