Welcome to the 1999 Symposium on VLSI Circuits

You are cordially invited to attend the 1999 Symposium on VLSI Circuits, to be held on June 17-19th 1999, at the Rihga Royal Hotel Kyoto in Kyoto, Japan.

The Symposium, now in its thirteenth year, has established itself as a major international forum for presenting and exchanging ideas on important new developments in the VLSI circuit design community. The scope of the Symposium has traditionally covered Analog, Digital, Memory, Signal Processing and Communications circuits with contributions from both industry and universities around the world.

Preceding the Symposium, on June 16th, a one-day Short Course on VLSI Circuits will be held. This short course will focus on ''System LSI and the Related Design Technology''.

As has been the tradition for a number of years, the Symposium on VLSI Circuits will be held for three days following the Symposium on VLSI Technology at the same location.

This year the program committee reviewed 146 papers submitted from 16 countries around the world and 52 papers were selected for presentation. We hope that these papers disclose new and interesting circuit design concepts for memories, processors, communication circuits, analog and signal processing. We expect the technical content of the program to make the Symposium a fruitful event for every attendee.

In addition, we have invited four distinguished speakers to describe recent advances and new challenges in VLSI circuits and technology.

For the first time, we offer a special joint session on Technology for System LSI, which will cover an important interface between circuits and technology. This session will be held on June 16, the last day of the Technology Symposium, and is open for attendance by those registering for either the Circuits Symposium or the Technology Symposium.

In contrast to these formal talks, we have prepared three evening rump sessions on interesting and provocative subjects that offer you an opportunity to participate in the discussions in an international environment. There is also a joint rump session with the Symposium on VLSI Technology on the evening of June 16th, the day before the Symposium on VLSI Circuits begins.

This booklet contains the advance program together with forms for the Symposium registration and hotel reservations. Please try to complete and return these forms as soon as possible. While on-site registration will be available, pre-registration will facilitate Symposium planning and hence is offered at significantly lowercost.

We look forward to meeting with you at the Symposium in Kyoto.

Masao Taguchi	David Scott
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1999 SYMPOSIUM ON VLSI CIRCUITS

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PROGRAM

Thursday, June 17

Session 1: Welcome and Plenary Session I [Shunju]

Chairpersons: M. Taguchi, *Fujitsu*
D. Scott, *Texas Instruments*

8:30 **1-1** **Welcome and Opening Remarks**
A. Iwata, *Hiroshima Univ.*
B. Bidermann, *Tripath Technology*

8:45 **1-2** **Asian Semiconductor Strategy for 21st Century (Invited)**
F.-C. Tseng, *Taiwan Semiconductor Manufacturing, Taiwan*

9:30 **1-3** **CMOS Technology; Present and Future (Invited)**
B. Davari, *IBM, USA*

(Break 10:15-10:35)

Session 2: Digital [Shunju]

Chairpersons: T. Kuroda, *Toshiba*
J. Alvarez, *Motorola*

10:35 **2-1** **A Low-Power DCT Core Using Adaptive Bitwidth and Arithmetic Activity Exploiting Signal Correlations and Quantization**
T. Xanthopoulos and A. Chandrakasan
Massachusetts Institute of Technology, USA

11:00 **2-2** **A 1V, 10.4mW Low Power DSP core for Mobile Wireless Use**
T. Shiota, I. Fukushi, R. Ohe, W. Shibamoto, M. Hamaminato, R. Sasagawa, A. Tsuchiya, T. Ishihara and S. Kawashima
Fujitsu Laboratories Limited, JAPAN

11:25 **2-3** **A Compact 54×54-bit Multiplier with Improved Wallace-Tree Structure**
N. Itoh, Y. Naemura*, H. Makino and Y. Nakase
*Mitsubishi Electric Corporation and *Mitsubishi Electric Engineering Company Limited, Japan*

11:50 **2-4** **A 250MHz CMOS Floating-Point Divider with Operand Pre-Scaling**
S. Inui, T. Uesugi, H. Saito, Y. Hagihara, A. Yoshikawa, M. Nishida and M. Yamashina
NEC Corporation, JAPAN

(Lunch 12:15-13:45)

Session 3: High Speed Link I [Shunju]

Chairpersons: D.-K. Jeong, *Seoul National Univ.*
T. Haulin, *Ericsson Telecom*

13:45 **3-1** **A 50 Gb/s 32×32 CMOS Crossbar Chip using Asymmetric Serial Links**
K.-Y.K. Chang, S-T. Chuang, N. McKeown and M. Horowitz
Stanford University, USA

14:10 **3-2** **840 Mb/s CMOS Demultiplexed Equalizing Transceiver for DRAM-to-Processor Communication**
J.-Y. Sim, Y.-S. Sohn, H.-J. Park, C.-H. Kim* and S.-I. Cho*
*Pohang University of Science and Technology and *Samsung Electronics Co., Korea*

14:35 3-3 A Low-power Multi-gigabit CMOS/SIMOX LSI Design Using Two Power Supply Voltages
Y. Ohtomo, H. Sawada*, T. Ohno, Y. Sakakibara, Y. Sato, T. Ishihara, S. Matsuoka** and M. Shimaya
*NTT System Electronics Laboratories, *NTT Electronics Corp. and **NTT Network Service Laboratories, Japan*

15:00 3-4 A 3.6Gb/s 340mW 16:1 Pipe-Lined Multiplexer using SOI-CMOS Technology
T. Nakura, K. Ueda, K. Kubo, W. Fernandez, Y. Matsuda and K. Mashiko
Mitsubishi Electric Corp., Japan

(Break 15:25-15:45)

Session 4: Flash [Shunju]

Chairpersons: M. Hiraki, *Hitachi*
S. Borkar, *Intel*

13:45 4-1 Charge Sharing Concept for Power Efficiency and EME Improvement of Boosted Charge Pumps in NVMs
C. Lauterbach, W. Weber, D. Römer and M. Huber*
*Siemens AG and *Technische Universität München, Germany*

14:10 4-2 A Sampling Weak-Program Method to Tighten Vth-distribution of 0.5V for Low-Voltage Flash Memories
H. Shiga, T.Tanzawa, A. Umezawa, T. Taura, T. Miyaba*, M.Saito, S. Kitamura, S. Mori and S. Atsumi
*Toshiba Corporation and *Toshiba Microelectronics Corporation, Japan*

14:35 4-3 A Source-line Programming Scheme for Low Voltage Operation NAND Flash Memories
K. Takeuchi, S. Satoh, K. Imamiya, Y. Sugiura, H. Nakamura, T. Himeno, T. Ikehashi, K. Kanda, K. Hosono and K. Sakui
Toshiba Corporation, Japan

15:00 4-4 A 144Mb 8-Level NAND Flash Memory with Optimized Pulse Width Programming
H. Nobukata, S. Takagi, K. Hiraga, T. Ohgishi, M. Miyashita, K. Kamimura, S. Hiramatsu, K. Sakai, T. Ishida, H. Arakawa, M. Itoh, I. Naiki and M. Noda
Sony Corporation, Japan

(Break 15:25-15:45)

Session 5: High Speed Link II [Shunju]

Chairpersons: M. Yamashina, *NEC*
M. Izzard, *Texas Instruments*

15:45 5-1 A 0.3-μm CMOS 8-Gb/s 4-PAM Serial Link Transceiver
R. Farjad-Rad, C.-K.K. Yang, M. Horowitz and T. Lee
Stanford University, USA

16:10 5-2 An Integratable 1-2.5Gbps Low Jitter CMOS Transceiver with Built in Self Test Capability
A.-L. Yee, R. Gu, H.-C. Lin, A. Tsong, R. Prentice, J. Tran*, R. Venett, S. Spencer, V. Pathak, E. Suder and M. Izzard
*Texas Instruments Inc. and *Sun MicroSystems Inc., USA*

16:35 5-3 A 1Gbps Transceiver with Receiver-End Deskewing Capability using Non-Uniform Tracked Oversampling and a 250-750MHz Four-Phase DLL
Y. Moon and D.-K. Jeong
Seoul National University, Korea

17:00 5-4 GAD: A 12-GS/s CMOS 4-bit A/D Converter for an Equalized Multi-Level Link
W. Ellersick, C.-K.K. Yang, M. Horowitz and W. Dally
Stanford University, USA

Session 6: Analog [Shunju]

Chairpersons: Y. Sugimoto, *Chuo Univ.*
L. DeVito, *Analog Devices*

15:45 6-1 Wide Tuning Range Inversion-Mode Gated Varactor and Its Application on a 2-GHz VCO
W. Wong, F. Hui, Z. Chen, K. Shen and J. Lau
The Hong Kong University of Science & Technology, Hong Kong

16:10 6-2 1.5 V 10-12.5 GHz Integrated CMOS Oscillators
T.-P. Liu
Bell Laboratories, Lucent Technologies, USA

16:35 6-3 On-chip active guard band filters to suppress substrate-coupling noise in analog and digital mixed-signal integrated circuits
K. Makie-Fukuda and T. Tsukada
Hitachi Ltd., Japan

17:00 6-4 A High-Voltage Output Buffer Fabricated on a 2V CMOS Technology
L.T. Clark
Intel Corp., USA

20:00 Rump Sessions:

Organizer: Y. Sugimoto, *Chuo Univ.*

R-1 How to Break the Verification Bottleneck? Simulation vs. Emulation vs. ????ation?

Organizers: K. Asada, *Univ. of Tokyo*
Bill Carter, *Xilinx*

With today's semiconductor process technology it is possible to build very complex chips. In many cases the design is the easy part. The most difficult problem is how to verify that the design performs the desired function. It is not uncommon for verification engineers to outnumber design engineers on a complex project by a factor of five.

Traditionally, simulation was the sole tool used to verify proper circuit behavior prior to fabrication. But the level of integration possible today makes using only simulation impractical. It takes too long to do exhaustive testing using simulation alone. New tools and techniques have emerged to help solve this problem; each with its own advantages and disadvantages.

One method to improve simulation time is to use hardware simulation acceleration. In this case the some of the simulation algorithm is implemented in dedicated hardware to improve simulation time over a pure software implementation.

Another method is to emulate the design. In this case the netlist of the design is mapped into flexible hardware, commonly an array of Field Programmable Gate Arrays (FPGA's) and programmable interconnect chips. This allows the design to interface to external hardware and to be exercised at hardware rates, although typically much slower than the final silicon implementation.

Another technique to accelerate verification is to build a hardware prototype of the netlist in an FPGA or a fast turn ASIC. This allows even faster operation than emulation, but may require that the netlist be retargeted to the ultimate implementation technology

The use of pre-verified intellectual property (IP) is another way to minimize the verification bottleneck. This eliminates most of the verification effort since the IP is

"known good."

A new verification method that is gaining popularity is formal verification. In this method mathematical techniques are used to prove that two circuit descriptions have the same behavior. Circuits can be described as a netlist or in behavioral VHDL.

This panel will include proponents of several of these alternative solutions, as well as the ultimate judge, designers of complex chips, the users of the tools.

R-2 Future Logic: Synchronous or Asynchronous?

Moderators: K. Uchiyama, *Hitachi*
G. Taylor, *Intel*

With asynchronous microprocessors approaching commercial reality while RAMs are moving from asynchronous to synchronous interfaces, is asynchronous logic in our future? Is asynchronous logic the answer to clock distribution and synchronization problems? Will it help to control the power dissipation of microprocessors? Or will the lack of tools and design methodologies hamper its use?

Synchronization of large systems is increasingly difficult. Wiring pitches are shrinking on fixed size die while operating frequencies increase. As a result, the width of systems measured in clock cycles to cross a die is rapidly increasing. At the same time clock distribution and clocking latches with unchanged data consumes a significant amount of power. Is it reasonable to maintain synchronization across these distances, or is there a better way? Can we save the power dissipated synchronizing the system?

On the other hand, industry has a great deal of experience in dealing with synchronous systems. Are we ready to replace this? When will commercial design tools and environments be available for asynchronous logic? How will asynchronous design paradigms impact HDL's, synthesis, and timing? How will systems be validated, bugs reproduced, and issues debugged? Will performance equal that of synchronous design, and can it be guaranteed (a spinning disk drive can't be paused)?

The panel will address these and other questions to help the audience better understand asynchronous design and systems, and where they may appear in our future.

R-3 Low Voltage CMOS Analog Circuits - How low can we go?

Moderators: T. Tsukahara, *NTT*
G. Nasserbakht, *Proxim*

Scaled technologies progressively require lower supply voltages. While this is a blessing for most digital circuits, it poses significant challenges for analog design. It is not obvious if analog circuits can or should continue to co-exist with digital circuits on the same substrate and suffer from continued voltage scaling. So, is the solution "smarter" analog designers who can keep up with the sliding voltages and can continue to deliver high-performance analog circuits with sub 1V supplies, enabling the march towards true "system-on-chip" solutions? Or do we need "smarter" scaled technologies that can handle higher supply voltages? If so, is anybody going to pay for them? Or has the time come to abandon the "all-on-one-chip" fantasy and keep the analog circuits on more mature technologies and let the digital designers ride the technology scaling bandwagon alone? The answer may be different for different application areas (all analog circuits are not created equal). The panel is going to address the implications of further voltage scaling on various analog IC circuits and make predictions as to how low we can/should go.

Technology and Circuits Joint Rump Session

17:30-19:30

SOI: what are the roadblocks, if any, to become a mainstream technology?

Moderators: L. DeVito, *Analog Devices*
M. Yoshimi, *Toshiba*
J. Woo, *UCLA*

A number of companies have announced that they will employ SOI in actual LSI production. Have the issues all been settled? We would like to promote discussion among circuit designers and device/process engineers who are (or are not) interested in introducing SOI, focusing on the question ''Will SOI become a mainstream technology?''

Topics we would like to discuss include:

+ Will SOI analog/RF devices offer significant advantages over bulk Si technology?
+ Can SOI-MPUs exceed bulk Si MPUs in performance or not?
+ Can partially-depleted devices maintain advantages in very-low-power applications?
+ How can we downscale fully-depleted MOSFETs?
+ Will SOI DRAMs appear in the market?
+ How should we do with SOI design tools?
+ What is the reliability of SOI wafers?

*This session will be held on Wednesday, June 16

Friday, June 18

Session 7: Plenary Session II [Shunju]

Chairpersons: M. Taguchi, *Fujitsu*
D. Scott, *Texas Instruments*

8:30 **7-1** **10-100 Gb/s Throughput CMOS Techniques (Invited)**
C. Svensson and A. Edman, *Linkoping University, Sweden*

9:15 **7-2** **Technical Trends of LSI Packaging (Invited)**
S. Wakabayashi, *Shinko Electric Ind., Japan*

(Break 10:00-10:20)

Session 8: A/D, D/A Converters [Shunju]

Chairpersons: T. Miki, *Mitsubishi Electric*
T. Haulin, *Ericsson Telecom*

10:20 **8-1** **A 10b, 400 MS/s Glitch-Free CMOS D/A Converter**
K. Khanoyan, F. Behbahani and A.A. Abidi
University of California, USA

10:45 **8-2** **An 8b 500MS/s Full Nyquist Cascade A/D Converter**
K. Irie, N. Kusayanagi, T. Kawachi, T. Nishibu and Y. Matsumori
Yokogawa Electric Corporation, Japan

11:10 **8-3** **A 1V 6b 50MHz Current-Interpolating CMOS ADC**
B.-S. Song, M.-J. Choe, P. Rakers* and S. Gillig*
*University of Illinois and *Motorola Corporate R&D, USA*

11:35 **8-4** **An 8b 100MSample/s CMOS Pipelined Folding ADC**
M.-J. Choe, B.-S. Song and K. Bacrania*
*University of Illinois and *Harris Semiconductor, USA*

(Lunch 12:00-13:30)

Session 9: Wireless IC [Shunju I]

Chairpersons: M. Ishikawa, *DENSO*
A. Abidi, *Univ. of California*

13:30 9-1 CMOS 10 MHz-IF Downconverter with On-Chip Broadband Circuit for Large Image-Suppression
F. Behbahani, Y. Kishigami, J. Leete and A.A. Abidi
University of California, USA

13:55 9-2 A 12.4mW CMOS Front-End for a 5GHz Wireless-LAN Receiver
H. Samavati, H.R. Rategh and T.H. Lee
Stanford University, USA

14:20 9-3 A Wideband Bandpass Sigma-Delta Modulator for Wireless Applications
A. Tabatabaei and B.A. Wooley
Stanford University, USA

14:45 9-4 A Delta-Sigma True RMS-to-DC Converter Using an Indirect-Charge-Transfer Filter
W.-S. Wey and Y.-C. Huang
National Chiao Tung University, Taiwan, R.O.C.

(Break 15:10-15:30)

Session 10: FRAM and ROM [Shunju II]

Chairpersons: H. Yamauchi, *Matsushita Electric*
S. Borkar, *Intel*

13:30 10-1 High-speed Cascode Sensing Scheme for 1.0 V Contact-programming Mask ROM
R. Sasagawa, I. Fukushi, M. Hamaminato and S. Kawashima
Fujitsu Laboratories Limited, Japan

13:55 10-2 A 3.3-V 4-Mb Nonvolatile Ferroelectric RAM with a Selectively-Driven Double-Pulsed Plate Read/Write-Back Scheme
Y. Chung, M.-K. Choi, S.-K. Oh, B.-G. Jeon and K.-D. Suh
Samsung Electronics Co., Ltd., Korea

14:20 10-3 A Robust 8F² Ferroelectric RAM Cell with Depletion Device (DeFeRAM)
G. Braun, H. Hoenigschmid*, T. Schlager** and W. Weber
*Siemens Corporate Technology, *Siemens Semiconductor Group, Germany and **Siemens Semiconductor Group, Austria*

14:45 10-4 Gain Cell Block Architecture for Gigabit-Scale Chain Ferroelectric RAM
D. Takashima, Y. Oowaki and I. Kunishima
TOSHIBA Corporation, JAPAN

(Break 15:10-15:30)

Session 11: SRAM and Register [Shunju I]

Chairpersons: T. Mori, *Fujitsu Labs.*
B. Gieseke, *AMD*

15:30 11-1 A 500 MHz, write-bypassed, 88-entry, 90-bit register file
M. Golden and H. Partovi
Advanced Micro Devices, USA

15:55 11-2 A 1.0ns Access 770MHz 36Kb SRAM Macro
T. Uetake, Y. Maki, T. Nakadai, K. Yoshida, M. Susuki and R. Nanjo
Fujitsu Ltd., Japan

16:20 **11-3** **A 550-ps Access, 900-MHz, 1-Mb ECL-CMOS SRAM**
H. Nambu, K. Kanetani, K. Yamasaki, K. Higeta, M. Usami, M. Nishiyama, K. Ohhata*, F. Arakawa*, T. Kusunoki*, K. Yamaguchi** and N. Homma***
*Hitachi Ltd., *Hitachi Device Engineering Co., Ltd., **Hitachi ULSI Systems Co., Ltd. and ***Hosei University, Japan*

(Dinner 19:00 - 21:00)

Session 12: Frequency Synthesizers [Shunju II]

Chairpersons: N. Ishihara, *NTT*
M. Horowitz, *Stanford Univ.*

15:30 **12-1** **A 5GHz, 32mW CMOS Frequency Synthesizer With an Injection Locked Frequency Divider**
H.R. Rategh, H. Samavati and T.H. Lee
Stanford University, USA

15:55 **12-2** **A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-μm CMOS Technology**
C. Lam and B. Razavi
University of California, USA

16:20 **12-3** **A 2 V 150 MHz CMOS Digital Phase Modulator for Fast-Switching Frequency Synthesis**
W.-Z. Chen and J.-T. Wu
National Chiao-Tung University, Taiwan

(Dinner 19:00 - 21:00)

Saturday, June 19

Session 13: High Performance DRAM I [Shunju I]

Chairpersons: C.H. Kim, *Samsung Electronics*
P. Gillingham, *MOSAID*

8:30 **13-1** **A Precharged-Capacitor-Assisted Sensing (PCAS) Scheme with Novel Level Controller for Low Power DRAMs**
T. Kono, T. Hamamoto, K. Mitsui and Y. Konishi
Mitsubishi Electric Corporation, Japan

8:55 **13-2** **A 7F^2 Cell and Bitline Architecture Featuring Tilted Array Devices and Penalty-Free Vertical BL Twists for 4Gb DRAM's**
H. Hoenigschmid, A. Frey*, J. DeBrosse**, T. Kirihata**, G. Mueller, G. Daniel, G. Frankowsky, K. Guay**, D. Hanson**, L. Hsu**, B.Ji**, D. Netis**, S. Panaroni**, C. Radens**, A. Reith, D. Storaska**, H. Terletzki, O. Weinfurtner, J. Alsmeier, W. Weber* and M. Wordeman**
*Siemens Microelectronics,USA, *Siemens Central Technology, Germany and **IBM, USA*

9:20 **13-3** **A Pseudo Multi-Bank DRAM with Categorized Access Sequence**
S. Shiratake, K. Tsuchida, H. Toda, H. Kuyama, M. Wada, F. Kouno, T. Inaba, H. Akita and K. Isobe
TOSHIBA Corporation, Japan

9:45 13-4 A DRAM System for Consistently Reducing CPU Wait Cycles
Y. Kanno, H. Mizuno and T. Watanabe
Hitachi, Ltd., Japan

(Break 10:10-10:30)

Session 14: Image Sensor [Shunju II]

Chairpersons: K. Kotani, *Tohoku Univ.*
L.D. McIlrath, *Northeastern Univ.*

8:30 14-1 100.000 Pixel 120dB Imager in TFA-Technology
T. Lulé, H. Keller, M. Wagner and M. Böhm
Silicon Vision GmbH, Germany

8:55 14-2 A High Speed, 500 frames/s, 1024 x 1024 CMOS Active Pixel Sensor
A. Krymski, D. V. Blerkom, A. Andersson, N. Bock, B. Mansoorian, E.R. Fossum
Photobit Corporation, USA

9:20 14-3 A CMOS Imager with New Focal-Plane Motion Detectors
F. Okamoto, Y. Fujimoto, T. Nagata, M. Furumiya, K. Hatano, Y. Nakashiba and M. Yotsuyanagi
NEC Corporation, Japan

9:45 14-4 A Smart CMOS Imager with Pixel Level PWM Signal Processing
M. Nagata, M. Homma, N. Takeda, T. Morie and A. Iwata
Hiroshima University, Japan

(Break 10:10-10:30)

Session 15: High Performance DRAM II [Shunju I]

Chairpersons: C.H. Kim, *Samsung Electronics*
P. Gillingham, *MOSAID*

10:30 15-1 Embedded DRAM for a Reconfigurable Array
S. Perissakis, Y. Joo*, J. Ahn*, A. DeHon and J. Wawrzynek
*University of California, USA and *LG Semicon, Korea*

10:55 15-2 Dynamically Shift-Switched Dataline Redundancy Suitable for DRAM Macro with Wide Data Bus
T. Namekawa, S. Miyano, R. Fukuda, R. Haga, O. Wada, H. Banba, S. Takeda, K. Suda*, K. Mimoto, S. Yamaguchi**, T. Ohkubo**, H. Takato and K. Numata
*Toshiba Corporation, *Toshiba Microelectronics Corporation and **Toshiba Information Systems Corporation, Japan*

11:20 15-3 A Multiple Vendor 2.5-V DLL for 1.6-GB/s RDRAMs
C. Portmann, A. Chu, N. Hays, S. Sidiropoulos, D. Stark, P. Chau, K. Donnelly and B. Garlepp
Rambus Inc., USA

(11:45 Closing)

Session 16: Finger Print Sensor [Shunju II]

Chairpersons: M. Ikeda, *Univ. of Tokyo*
A. Chandrakasan, *MIT*

10:30 **16-1** **A High-Resolution Capacitive Fingerprint Sensing Scheme with Charge-Transfer Technique and Automatic Contrast Emphasis**
H. Morimura, S. Shigematsu and K. Machida*
*NTT Integrated Information & Energy Systems Laboratories and *NTT System Electronics Laboratories, Japan*

10:55 **16-2** **CMOS Fingerprint Sensor with Automatic Local Contrast Adjustment and Pixel-Parallel Encoding Logic**
S. Jung, R. Thewes, T. Scheiter, K. Goser* and W. Weber
*Siemens AG and *University of Dortmund, Germany*

(11:20 Closing)

Joint Session

Wednesday, June 16

Technology for System LSI
(Technology and Circuits Joint Session) [Shunju]

Chairpersons: T.M. Liu, *TSMC*
M. Horowitz, *Stanford Univ.*

15:30 **J-1** **Future perspective and scaling down roadmap for RF CMOS**
E. Morifuji, H.S. Momose, T. Ohguro, T. Yoshitomi, H. Kimijima, F. Matsuoka, M. Kinugawa, Y. Katsumata and H. Iwai
Toshiba Corporation, Japan

15:55 **J-2** **Compact Distributed RLC Models for Multilevel Interconnect Networks**
J.A. Davis and J.D. Meindl
Georgia Institute of Technology, USA

16:20 **J-3** **Micro IDDQ Test using Lorentz Force MOSFET's**
K. Nose and T. Sakurai
University of Tokyo, Japan

16:45 **J-4** **Monte Carlo Modeling of Threshold Variation due to Dopant Fluctuations**
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