Welcome to the 1999 Symposium on VLSI Technology

On behalf of the organizing Committees, we invite you to attend the 1999 Symposium on VLSI Technology to be held from June 14–16 in Kyoto, Japan.

The 1999 Symposium promises to be exciting. Over 200 excellent papers were submitted from all over the world. From this impressive roster, we have selected 79 contributed papers organized into 20 sessions including a session for 4 highlight papers. We are also delighted to have two distinguished Invited Speakers for the Plenary Session. Mr. Yoshiaki Kushiki, director of Multimedia Development Center of Matsushita, will speak on the Digital Consumer Electronics Evolution in the Multimedia and Network Age. Mr. Daniel T. Niles from BancBoston Roberstson Stephens will speak on the Economic Trends in the Semiconductor Business. Further, we will have a joint special session on ''Technology for System LSI'' in the afternoon of Wednesday, June 16, which will be of great interest to both technology and circuit engineers. Any Circuits Symposium registrant can attend the joint special session.

Three regular Rump Sessions and one Joint Rump Session are planned for the evening of June 15th and 16th, respectively, as means to facilitate informal discussions among researchers. The Joint Session with the Symposium on VLSI Circuits will address ''Silicon On Insulator (SOI).'' The three regular Rump Sessions will cover specific technology-related topics of timely interest:

1) Technology Challenges for Scaled Cu/Low-k Interconnects
2) Gate Insulator; Hi-k vs. SiO_2
3) Flash vs. FeRAM; Which is the real winner ?

A one-day Short Course, planned for Sunday June 13, will cover ''Embedded Technologies for System on a Chip.'' This should be an excellent opportunity for experienced as well as young engineers to broaden their technical base.

The Symposium registration fee covers all of the sessions including the Rump Sessions. Daily continental breakfasts and the dinner are also included. Registration for the Short Course is extra. Information on the detailed registration fees and hotel reservation schedules is included in the Advance Program.

As in past years, we expect a strong participation from leaders in the VLSI industry as well as academic researchers. We look forward to an exciting Symposium in Kyoto. Please join us.

Masakazu Kakumu	Craig Lage
Program Chairman	Program Co-Chairman

1999 SYMPOSIUM ON VLSI TECHNOLOGY

Symposium Chairman:	
Masao Fukuma	NEC
Symposium Co-Chairman:	
Tony Alvarez	Cypress Semiconductor
Program Chairman:	
Masakazu Kakumu	Toshiba
Program Co-Chairman:	
Craig Lage	Motorola
Secretary:	
Takemitsu Kunio	NEC
(Publicity)	
Bob Havemann	Texas Instruments
Publications/Publicity:	
Makoto Ohkura	Hitachi
(Publications)	
Wah Kit Loh	Texas Instruments
Treasurer:	
Shinsuke Konaka	NTT
Richard Jaeger	Auburn Univ.
Local Arrangements:	
Yasuo Inoue	Mitsubishi Electric
Shoichiro Matsumoto	Sanyo Electric
Yuan Taur	IBM
Short Course Organizer:	
Tadashi Nishimura	Mitsubishi Electric
Simon Wong	Stanford Univ.

EXECUTIVE COMMITTEES

Japan Society of Applied Physics

Chairman:

Takuo Sugano	Toyo Univ.

Members:

Chun-Yen Chang	National Chiao Tung Univ.
Yutaka Hayashi	Sony
Chang-Gyu Hwang	Samsung Electronics
Hajime Ishikawa	Fujitsu Labs.
Choong-Ki Kim	KAIST
Susumu Kohyama	Toshiba
Yojiro Mano	Matsushita Electric
Toshiaki Masuhara	Hitachi
Akihiko Morino	NEC
Tadashi Nishimura	Mitsubishi Electric
Eiji Takeda	Hitachi
Ken Takeya	NTT
Fang-Churng Tseng	TSMC

IEEE

Chairman:

James T. Clemens	Bell Labs., Lucent Technologies

Members:

Asad Abidi	Univ. of California
Tony Alvarez	Cypress Semiconductor
Dirk Bartelink	Hewlett Packard
Bill Bidermann	Tripath Technology
Richard Chapman	Texas Instruments
Gilbert Declerck	IMEC
Youssef El-Mansy	Intel
Richard Jaeger	Auburn Univ.
Nino Masnari	North Carolina State Univ.
Yoshi Nishi	Texas Instruments
Kevin O'Connor	Bell Labs., Lucent Technologies
Bill Siu	Intel
Charles Sodini	MIT
Peter Verhofstadt	Semiconductor Research
Ian Young	Intel

TECHNICAL PROGRAM COMMITTEES

JAPAN/FAR EAST

Chairman:

Masakazu Kakumu	Toshiba

Members:

Takahisa Eimori	Mitsubishi Electric
Hiroshi Hanafusa	Sanyo Electric
Jiro Ida	Oki Electric
Seiichiro Kawamura	Fujitsu
Masaaki Kinugawa	Toshiba
Shinsuke Konaka	NTT
Takemitsu Kunio	NEC
Sang-In Lee	Samsung Electronics
Teyin Mark Liu	TSMC
Shinji Odanaka	Matsushita Electronics
Makoto Ohkura	Hitachi
Yasuhisa Omura	Kansai Univ.
Shigeo Onishi	Sharp
Norikazu Ouchi	Sony
Kentaro Shibahara	Hiroshima Univ.
Tadashi Shibata	Univ. of Tokyo
Eiichi Suzuki	Electrotechnical Lab.

NORTH AMERICA/EUROPE

Chairman:

Craig Lage	Motorola

Members:

William H. Arnold	ASM Lithography
Mark T. Bohr	Intel
Guillermo Bomchil	France Telecom
Min Cao	Hewlett-Packard Labs.
T.C. Chen	IBM
Michael Chern	Atmel
Ludo Deferm	IMEC
Roger DeKeersmaecker	IMEC
Chuck Dennison	Micron Technology
Giorgio De Santi	SGS-Thomson Microelectronics
Bob Havemann	TI/SEMATECH
David Kyser	Advanced Micro Devices
Jack Lee	Univ. of Texas
Reinhard Mahnkopf	Siemens Microelectronics
Romek Nowak	Applied Materials
Carl Osburn	North Carolina State Univ.
Chien-Shing Pai	Lucent Technologies Bell Labs.
Rajat Rakkhit	LSI Logic
Jim Sansbury	Altera
Tom Seidel	Genus
Lisa Su	IBM
Yuan Taur	IBM
Jeff Watt	Cypress Semiconductor
Simon Wong	Stanford Univ.
Jason Woo	Univ. of California
Carel van der Poel	Philips Research Labs.

PROGRAM

Monday, June 14

Session 1: Welcome and Plenary Session [Shunju]

Chairpersons: M. Kakumu, *Toshiba*
C. Lage, *Motorola*

8:30 1-1 Welcome and Opening Remarks
M. Fukuma, *NEC*
T. Alvarez, *Cypress Semiconductor*

8:45 1-2 Digital Consumer Electronics Evolution in the Multimedia and Network Age (Invited)
Y. Kushiki, *Matsushita, Japan*

9:25 1-3 Economic Trends in the Semiconductor Business (Invited)
D.T. Niles, *BancBoston Roberstson Stephens, USA*

(Break 10:05-10:25)

Session 2: Highlights [Shunju]

Chairpersons: N. Ouchi, *Sony*
R. DeKeersmaecker, *IMEC*

10:25 2-1 High Performance 50-nm Physical Gate Length pMOSFETs by using Low Temperature Activation by Re-Crystallization Scheme
K. Tsuji, K. Takeuchi and T. Mogami
NEC, Japan

10:50 2-2 A 0.18 μm CMOS Logic Technology with Dual Gate Oxide and Low-k Interconnect for High-
Performance and Low-Power Applications.
C.H. Diaz, K.L. Young, J.H. Hsu, J.C.H. Lin, C.S. Hou, C.T. Lin, J.J. Liaw, C.C. Wu, C.W. Su, C.H. Wang, J.K. Ting, S.S. Yang, K.Y. Lee, S.Y. Wu, C.C. Tsai, H.J. Tao, S.M. Jang, S.L. Shue, H.C. Hsieh, Y.Y. Wang, C.C. Chen, S.C. Yang, S. Fu, S.Z. Chang, T.C. Lo, J.Y. Wu, J.S. Shy, C.W. Liu, S.H. Chen, B.L. Lin, B.K. Liew, T. Yen, C.H. Yu, Y.C. Chao, M.S. Liang, C. Wang and J.Y.C. Sun
Taiwan Semiconductor Manufacturing Company, Taiwan R.O.C.

11:15 2-3 Novel integration technology with Capacitor Over Metal(COM) by using Self-Aligned Dual Damascene(SADD) process for 0.15 μm stand-alone and embedded DRAMs
W.S. Yang, Y.K. Kim, S.H. Shin, W.S. Lee, K.H. Lee, H.S. Jeong, J.H. Lee, T.Y. Chung, H.S. Park, S.I. Lee, K. Kim, M.Y. Lee and C.G. Hwang
Samsung Electronics Co., Korea

11:40 2-4 A 0.22 μm CMOS-SOI Technology with a Cu BEOL
A. Ajmera, J.W. Sleight, F. Assaderaghi, R. Bolam, A. Bryant, M. Coffey, H. Hovel, J. Lasky, E. Leobandung, W. Rausch, D. Sadana, D. Schepis, L.F. Wagner, K. Wu, B. Davari and G. Shahidi
IBM Semiconductor Research and Development Center (SRDC), USA

(Lunch 12:05-13:30)

Session 3A: Flash Memory [Shunju I]

Chairpersons: T. Kunio, *NEC*
C. van der Poel, *Philips Research Labs.*

13:30 3A-1 **A Low Voltage Erase Technique for DINOR Flash Memory Devices**
Z. Liu and T.P. Ma
Yale University, USA

13:55 3A-2 **A Novel High Performance and Reliability p-Type Floating Gate N-Channel Flash EEPROM**
S.S. Chung, C.M. Yih, S.T. Liaw, Z.H. Ho, S.S. Wu, C.J. Lin*, D.S. Kuo* and M.S. Liang*
*National Chiao Tung University and *Tsmc, Taiwan*

14:20 3A-3 **A 0.9V Operation 2-Transistor Flash Memory for Embedded Logic LSIs**
K. Takahashi, H. Doi, N. Tamura, K. Mimuro, T. Hashizume, Y. Moriyama and Y. Okuda
Matsushita Electronics Corporation, Japan

14:45 3A-4 **Suppression of Anomalous Leakage Current in Tunnel Oxides by Fluorine Implantation to Realize Highly Reliable Flash Memory**
M. Ushiyama, A. Satoh and H. Kume
Hitachi Ltd., Japan

(Break 15:10-15:30)

Session 3B: SOI Technology [Suzaku II]

Chairpersons: S. Kawamura, *Fujitsu*
J. Woo, *Univ. of California*

13:30 3B-1 **0.18 μm Metal Gate Fully-Depleted SOI MOSFETs for Advanced CMOS Applications**
J. Chen, B. Maiti, D. Connelly, M. Mendicino, F. Huang, O. Adetutu, Y. Yu, D. Weddington, W. Wu, J. Candelaria, D. Dow, P. Tobin and J. Mogab
Motorola, USA

13:55 3B-2 **Minimizing Body Instability in Deep Sub-micron SOI MOSFETs for Sub-1V RF Applications**
Y.-C. Tseng, W.M. Huang*, M. Mendicino*, P. Welch*, V. Ilderem* and J.C.S. Woo
*University of California and *Motorola Inc., USA*

14:20 3B-3 **SON (Silicon On Nothing) - A NEW DEVICE ARCHITECTURE FOR THE ULSI ERA.**
M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen*, J.-L. Regolini, C. Morin, A. Schiltz, J. Martins*, R. Pantel and J. Galvier
*France Telecom and *ST Microelectronics, France*

14:45 3B-4 **High Performance Fully and Partially Depleted Poly-Si Surrounding Gate Transistors**
H.-J. Cho and J.D. Plummer
Stanford University, USA

(Break 15:10-15:30)

Session 4A: DRAM Technology I [Shunju I]

Chairpersons: S.-I. Lee, *Samsung Electronics*
S. Wong, *Stanford Univ.*

15:30 4A-1 **A DRAM technology using MIM BST capacitor for 0.15 μm DRAM generation and beyond**
K.N. Kim, D.H. Kwak, Y.S. Hwang, G.T. Jeong, T.Y. Chung, B.J. Park, Y.S. Chun, J.H. Oh, C.Y. Yoo and B.S. Joo
Samsung Electronics Co., Korea

15:55 4A-2 **Aluminum Word Line and Bit Line Fabrication Technology for COB DRAM Using a Polysilicon-Aluminum Substitute**
S. Nakamura, R. Suzuki, M. Fukuda, M. Kobayashi and A. Hatada
Fujitsu Laboratories Ltd., Japan

16:20 4A-3 **A New Process Integration - P^3 (Pre Poly Plug) - for Giga Bit DRAM Era**
T. Yoon, K. Joung, J. Kim, W. Cho, W. Yang and D. Song
LG Semicon Co., Ltd., Korea

16:45 4A-4 **Highly Reliable MIM Capacitor Technology Using Low Pressure CVD-WN Cylinder Storage-Node for 0.12 μm-scale Embedded DRAM**
S. Kamiyama, J.M. Drynan, Y. Takaishi and K. Koyama
NEC Corporation, Japan

(Dinner 19:00 - 21:00)

Session 4B: Interconnect Technology [Suzaku II]

Chairpersons: S. Ohnishi, *Sharp*
C.-S. Pai, *Lucent Technologies Bell Labs.*

15:30 4B-1 **A Novel Clustered Hard Mask Technology for Dual Damascene Multilevel Interconnects with Self-Aligned Via Formation Using an Organic Low k Dielectric**
N. Aoi, E. Tamaoka, M. Yamanaka, S. Hirao, T. Ueda and M. Kubota
Matsushita Electronics Corporation, Japan

15:55 4B-2 **Slotted Vias for Dual Damascene Interconnects in 1Gb DRAMs**
R.F. Schnabel, G. Bronner*, L. Clevenger*, D. Dobuzinski*, G. Costrini*, R. Filippi*, J. Gambino*, M. Hug, R. Iggulden*, C. Lin, K.P. Muller*, G. Mueller, J. Nuetzel, C. Radens*, S. Weber and F. Zach*
*Siemens Microelectronics and *IBM Microelectronics, USA*

16:20 4B-3 **High Performance Cu Interconnects with Low-k BCB-polymers by Plasma-enhanced Monomer-vapor Polymerization (PE-MVP) method**
J. Kawahara, A. Nakano*, S. Saito, K. Kinoshita, T. Onodera and Y. Hayashi
*NEC Corporation and *ASM Japan K.K., Japan*

16:45 4B-4 **Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD**
M. Tanaka, S. Saida, T. Iijima and Y. Tsunashima
TOSHIBA corp., Japan

(Dinner 19:00 - 21:00)

Tuesday, June 15

Session 5A: Shallow Junction [Shunju I]

Chairpersons: J. Ida, *Oki Electric*
B. Havemann, *TI/SEMATECH*

8:30 5A-1 Co Salicide Compatible 2-step Activation Annealing Process for Deca-nano Scaled MOSFETs
K. Goto, Y. Sambonsugi and T. Sugii
Fujitsu Laboratories Ltd., Japan

8:55 5A-2 A source/drain formation technology utilizing sub-10 keV arsenic and assist-phosphorus implantation for 0.13 μm MOSFET
K. Imai, S. Shishiguchi, K. Yamaguchi, N. Kimizuka, H. Onishi and T. Horiuchi
NEC Corporation, Japan

9:20 5A-3 Improvement of $CoSi_2$ Stability on Fine Grain Sized Poly-Si Using Nitrogen Implantation Through Co Monosilicide and Its Effect on 0.18 μm Dual Gate CMOS
J.-U. Bae, D.K. Sohn, J.-S. Park, B.H. Lee, C.H. Han and J.J. Kim
LG semicon. Co. Ltd., Korea

9:45 5A-4 Low Resistance Co-Salicided 0.1 μm CMOS Technology Using Selective Si Growth
H. Sayama, S. Shimizu, Y. Nishida, T. Kuroi, Y. Kanda, M. Fujisawa, Y. Inoue, T. Nishimura, T. Oishi, T. Nakahata, T. Furukawa, S. Yamakawa, Y. Abe, S. Maruno, Y. Tokuda and S. Satoh
Mitsubishi Electric Corporation, Japan

(Break 10:10-10:30)

Session 5B: Dielectric Reliability [Suzaku II]

Chairpersons: Y. Omura, *Kansai Univ.*
R. Mahnkopf, *Siemens Microelectronics*

8:30 5B-1 A Concept of Gate Oxide Lifetime Limited by "B-mode" Stress Induced Leakage Currents in Direct Tunneling Regime
K. Okada, H. Kubo, A. Ishinaga and K. Yoneda
Matsushita Electronics Corporation, Japan

8:55 5B-2 Temperature acceleration of oxide breakdown and its impact on ultra-thin gate oxide reliability
R. Degraeve, N. Pangon, B. Kaczer, T. Nigam, G. Groeseneken and A. Naem*
*IMEC, Belgium and *National Semiconductor, USA*

9:20 5B-3 Dielectric Breakdown Mechanism of Thin-SiO_2 Studied by the Post-breakdown Resistance Statistics
H. Satake and A. Toriumi
Toshiba Corporation, Japan

9:45 5B-4 C-V and Gate Tunneling Current Characterization of Ultra-Thin Gate Oxide MOS (t_{ox} = 1.3-1.8nm)
C.-H. Choi, J.-S. Goo, T.-Y. Oh, Z. Yu, R.W. Dutton, A. Bayoumi*, M. Cao*, P.V. Voorde* and D. Vook*
*Stanford University and *HP Co., USA*

(Break 10:10-10:30)

Session 6A: Channel Engineering [Shunju I]

Chairpersons: S. Odanaka, *Matsushita Electronics*
M.T. Bohr, *Intel*

10:30 6A-1 **An Efficient Lateral Channel Profiling of Poly-SiGe-Gated PMOSFET's for 0.1 μm CMOS Low-Voltage Applications**
Y.V. Ponomarev, P.A. Stolk, A.C.M.C. van Brandenburg, C.J.J. Dachs, M. Kaiser, A.H. Montree, R. Roes, J. Schmitz and P.H. Woerlee
Philips Research Laboratories, The Netherlands

10:55 6A-2 **Indium Tilted Channel Implantation Technology for 60nm nMOSFET**
Y. Momiyama, S. Yamaguchi*, S. Ohkubo and T. Sugii
*Fujitsu Laboratories Ltd. and *Fujitsu Ltd., Japan*

11:20 6A-3 **Channel Engineering for High Speed Sub-1.0V Power Supply Deep Sub-micron CMOS**
B. Cheng, A. Inani, R. Rao and J.C.S. Woo
University of California, USA

11:45 6A-4 **Channel Engineering for 0.2 μm Surface Channel pMOSFETs Using Electron Beam Irradiation**
J.M. Ha, S.H. Kim, W.S. Kim, S.P. Kim, J.-H. Ku, H.J. Lee, J.W. Park, K. Fujihara, H.K. Kang and M.Y. Lee
Samsung Electronics Co., Ltd., Korea

(Lunch 12:10-13:30)

Session 6B: Gate Dielectric I [Suzaku II]

Chairpersons: M. Ohkura, *Hitachi*
G. Bomchil, *France Telecom*

10:30 6B-1 **The impact on bias temperature instability for direct-tunneling ultra-thin gate oxide on MOSFET scaling**
N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai and T. Horiuchi
NEC Corporation, JAPAN

10:55 6B-2 **Severe Thickness Variation of Sub-3nm Gate Oxide Due to Si Surface Faceting, Poly-Si Intrusion, and Corner Stress**
C.T. Liu, F.H. Baumann, A. Ghetti, H.H. Vuong, C.P. Chang, K.P. Cheung, J.I. Colonell, W.Y.C. Lai, E.J. Lloyd, J.F. Miner, C.S. Pai, H. Vaidya, R. Liu and J.T. Clemens
Bell Labs, USA

11:20 6B-3 **Quantum Effect in Oxide Thickness Determination From Capacitance Measurement**
K. Yang, Y.-C. King and C. Hu
University of California, USA

11:45 6B-4 **100nm Channel Length MNSFETs using a Jet Vapor Deposited Ultra-thin Silicon Nitride Gate Dielectric**
S. Mahapatra, V.R. Rao, K.N. ManjulaRani, C.D. Parikh, J. Vasi, B. Cheng*, M. Khare** and J.C.S. Woo***
*Indian Institute of Technology, India, *Motorola, **Yale University and ***University of California, USA*

(Lunch 12:10-13:30)

Session 7A: Memory Technology [Shunju I]

Chairpersons: T. Shibata, *Univ. of Tokyo*
M. Cao, *Hewlett-Packard Labs.*

13:30 7A-1 Alpha-SER Modeling & Simulation for Sub-0.25 μm CMOS Technology
C. Dai, N. Hakim, S. Hareland, J. Maiz and S.-W. Lee
Intel Corporation, USA

13:55 7A-2 Substrate Enhanced Gate Current: Device Design and Temperature Impact and Disturbs in Programming Flash Memories with Negative Body Bias
R. Annunziata, T. Ghilardi and M. Tosi
STMicroelectronics, Italy

14:20 7A-3 Novel *Bi*-Directional Tunneling *NOR* (*BiNOR*) Type 3-D Flash Memory Cell
E.C.-S. Yang, C.-J. Liu, T.-S. Chao*, M.-C. Liaw* and C.C.-H. Hsu
*National Tsing-Hua University and *National Nano Device Laboratory, Taiwan, R.O.C.*

14:45 7A-4 A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure
F. Hayashi and J.D. Plummer*
*NEC Corporation, Japan and *Stanford University, USA*

(Break 15:10-15:30)

Session 7B: Advanced CMOS Technology I [Suzaku II]

Chairpersons: K. Shibahara, *Hiroshima Univ.*
Y. Taur, *IBM Research Center*

13:30 7B-1 65nm physical gate length NMOSFETs with heavy ion implanted pockets and highly reliable 2nm-thick gate oxide for 1.5V operation
C. Caillat, S. Deleonibus, G. Guegan, S. Tedesco, B. Dal'zotto, M. Heitzmann, F. Martin, P. Mur, B. Marchand* and F. Balestra*
*Laboratoire d'Electronique de Technologie et d'Instrumentation (LETI) and *Laboratoire de Physique des Composants à Semiconducteurs, FRANCE*

13:55 7B-2 Smart pockets - total suppression of roll-off and roll-up
R. Gwoziecki and T. Skotnicki
France Telecom, France

14:20 7B-3 0.1-μm CMOS with Shallow and Steep Source/Drain Extensions Fabricated by Using Rapid Vapor-phase Doping (RVD)
T. Uchino, Y. Kiyota and T. Shiba
Hitachi Ltd., Japan

14:45 7B-4 Work Function Controlled Metal Gate Electrode on Ultrathin Gate Insulators
K. Nakajima, Y. Akasaka, M. Kaneko*, M. Tamaoki, Y, Yamada, T. Shimizu, Y. Ozawa and K. Suguro
*Toshiba Corp. and *Toshiba Microelectronics Corp., Japan*

(Break 15:10-15:30)

Session 8A: DRAM Capacitor Technology [Shunju I]

Chairpersons: S.-I. Lee, *Samsung Electronics*
J. Watt, *Cypress Semiconductor*

15:30 8A-1 Inner Cylinder Ta_2O_5 Capacitor Process for 1Gb DRAM and beyond
S.J. Won, Y.W. Hyung, K.J. Nam, Y.D. Kim, K.Y. Park, Y.W. Park, S.I. Lee and M.Y. Lee
Samsung Electronics Co.,Ltd., Korea

15:55 8A-2 Leakage-current mechanism of a tantalum-pentoxide capacitor on rugged Si with a CVD-TiN plate electrode for high-density DRAMs
H. Miki, M. Kunitomo, R. Furukawa, T.Tamaru, H. Goto, S. Iijima, Y. Ohji, H. Yamamoto, J. Kuroda*, T. Kisu* and I. Asano
*Hitachi, Ltd. and *Hitachi ULSI Systems Co., Japan*

16:20 8A-3 In-situ Multi-Step (IMS) CVD Process of (Ba,Sr)TiO_3 using Hot Wall Batch Type Reactor for DRAM Capacitor Dielectrics
M. Kiyotoshi, S. Yamazaki, K. Eguchi, K. Hieda, Y. Fukuzumi, M. Izuha, T. Aoyama, S. Niwa, K. Nakamura, A. Kojima, H. Tomita, T. Kubota, M. Satoh, Y. Kohyama, Y. Tsunashima, T. Arikado and K. Okumura
Toshiba Corporation, Japan

16:45 8A-4 A Self-aligned Stacked Capacitor using Novel Pt Electroplating Method for 1 Gbit DRAMs and Beyond
H. Horii, B.T. Lee, H.J. Lim, S.H. Joo, C.S. Kang, C.Y. Yoo, H.B. Park, W.D. Kim, S.I. Lee and M.Y. Lee
Samsung Electronics Co., Ltd., Korea(ROK)

Session 8B: Advanced CMOS Technology II [Suzaku II]

Chairpersons: S. Odanaka, *Matsushita Electronics*
G. De Santi, *SGS-Thomson Microelectronics*

15:30 8B-1 A 0.18 μm High-Performance Logic Technology
S. Crowder, S. Greco, H. Ng, E. Barth, K. Beyer, G. Biery, J. Connolly, C. DeWan, R. Ferguson, M. Hargrove, E. Nowak, P. McLaughlin, R. Purtell, R. Logan, J. Oberschmidt, A. Ray, D. Ryan, K. Tallman, T. Wagner, V. McGahay, E. Crabbe, P. Agnello, R. Goldblatt, L. Su and B. Davari
IBM Semiconductor Research and Development Center (SRDC), USA

15:55 8B-2 A 0.10-μm CMOS Device with a 40-nm Gate Sidewall and Multilevel Interconnects for System LSI
H. Wakabayashi, T. Yamamoto, Y. Saito, T. Ogura, M. Narihiro, K. Tsuji, T. Fukai, K. Uejima, Y. Nakahara, K. Takeuchi, Y. Ochiai, T. Mogami and T. Kunio
NEC Corporation, Japan

16:20 8B-3 Realization of 0.1 μm Buried-Channel PMOSFETs by Device Restructuring Using Tilted Well Implantation Technology
T. Tanaka, Y. Momiyama, K. Goto, Y. Sambonsugi, M. Deura and T. Sugii
Fujitsu Laboratories Ltd., Japan

16:45 8B-4 Integration of 3 Level Air Gap Interconnect for Sub-quarter Micron CMOS
T. Ueda, K. Yamashita, E. Tamaoka, H. Sato, K. Egashira, N. Aoi and M. Ogura
Matsushita Electronics Corporation, JAPAN

20:00 Rump Sessions:

Organizers: M. Kinugawa, *Toshiba*
J. Woo, *Univ. of California*

R-1 Technology Challenges for Scaled Cu/Low k Interconnects
Moderators: N. Kobayashi, *Hitachi*
R. Havemann, *Sematech/TI*

Although copper interconnects have now been demonstrated on certain high performance products, significant technology challenges remain, including: Cu integration with low k dielectrics, scaling dual damascene structures and reliability of Cu/low k inter-

connects. In addition, the cost versus performance tradeoff, timing for insertion and target products are still unclear when comparing Cu with the more mature Al technology. This session will address the technical and strategic advantages and issues associated with the introduction of Cu/oxide and Cu/low k dielectrics with the goal of highlighting industry needs and timeline for Cu technology insertion.

R-2 Gate Insulator;Hi-k vs. SiO_2

Moderators: A. Toriumi, *Toshiba*
H. Huff, *Sematech*

The International Technology Roadmap for Semiconductors (ITRS) has monitored the evolution of the gate dielectric equivalent oxide thickness with technology node. The advent of ultra-thin dielectrics ($\leqq$1.5 nm equivalent oxide thickness)has exacerbated the measurement metrology, MOSFET off-state leakage and component reliability. These issues may be partially addressed by the utilization of single or multi-layer oxynitride stacks, eventually in conjunction with metal electrodes, although it is expected that the sub 70 nm node will be especially critical. In that regard, the possible utilization of high K gate dielectrics (and its relevant metal electrodes) is being explored as a possible solution. The thermal stability and stoichiometric control of K gate dielectric materials as well as their compatability with CMOS processing, however, has exemplified a host of significant scientific and technical challenges. For example, the increased thickness of the high K gate dielectric in conjunction with the decreasing channel length presents electrical design issues not heretofore relevant. Finally, the commercial availability of equipment and processes to support the viability of the high K era is in itself an arena worthy of a separate symposium. These and related issues will be briefly discussed during this brief panel discussion

R-3 Flash vs. FeRAM Which is the real winner?

Moderators: S. Ohnichi, *Sharp*
P. Cappelletti, *STMicroelectroncis*

Logic embedded non-volatile memories are actively developed to achieve the mobile communication tools with high performance. Flash-EEPROMs have been widely used as programmable memories mainly for Personal handy-phone. By increasing memory densities above 32Mbits, they will be applied for the data storage of the products such as CD-ROM, digital steel camera and so on.

FeRAMs from 4kbits to 64kbits are produced now. They have several excellent specifications such as low voltage operation and high endurance with high speed. These properties are very applicable for the contactless IC-Cards and the Smart Cards, which market will increase radically in the year 2000.

We will discuss which device is the real winner for future non-volatile memories, and the possibility of coexistence between FeRAMs and Flash memories.

1) IC-cards including Mbits non-volatile memories will be required in the near future. Considering from the cost performance, is it possible for FeRAMs to compete with Flash memories?
2) FeRAMs have some advantages regarding to endurance, speed and low voltage operation in comparison with Flash memories. What are really valuable applications and products to make good use of these specifications?
3) Flash memories have the possibilities to obtain lower voltage operation and faster programming/ erasing speed. What are the attainable specifications and desirable values to develop new market?

Wednesday, June 16

Session 9A: Gate Dielectric II [Shunju I]

Chairpersons: E. Suzuki, *Electrotechnical Lab.*
L. Su, *IBM SRDC*

8:30 9A-1 **High-integrity Ultra-thin Silicon Nitride Film Grown at Low Temperature for Extending Scaling Limit of Gate Dielectric**
K. Sekine, Y. Saito, M. Hirayama and T. Ohmi
Tohoku University, Japan

8:55 9A-2 **High Performance & Highly Reliable Deep Submicron CMOSFETs using Nitrided-Oxide**
K. Irino, Y. Tamura, S. Ohkubo, T. Nakanishi, M. Shigeno, K. Hikazutani*, M. Higashi*, T. Fukuda* and K. Takasaki
*Fujitsu Laboratories Ltd. and *FUJITSU LIMITED, Japan*

9:20 9A-3 **Improvement of 1/f noise by using VHP (Vertical High Pressure) oxynitride gate insulator for deep-sub micron RF and analog CMOS**
H. Kimijima, T. Ohguro, B. Evans*, B. Acker*, J. Bloom*, H. Mabuchi*, D.-L. Kwong**, E. Morifuji, T. Yoshitomi, H.S. Momose, M. Kinugawa, Y. Katsumata and H. Iwai
*Toshiba Corporation, Japan, *GaSonics International and **University of Texas at Austin, USA*

9:45 9A-4 **New Optimization Guidelines for Sub-0.1 μm CMOS Technologies with 2 nm NO Gate Oxynitrides**
M. Fujiwara, M. Takayanagi and Y. Toyoshima
Toshiba Corporation, Japan

(Break 10:10-10:30)

Session 9B: Process Technology [Shunju II]

Chairpersons: H. Hanafusa, *Sanyo Electric*
T. Seidel, *Genus*

8:30 9B-1 **Node connection / quantum phase-shifting mask --- Path to below 0.3-um pitch, proximity effect free random interconnect and memory patterning**
H. Fukuda
Hitachi Ltd., Japan

8:55 9B-2 **New Radical Injection Method for High-Performance and Chargeless Dielectric Etching**
S. Samukawa, T. Mukai and K. Noguchi
NEC Corporation, Japan

9:20 9B-3 **Balanced Electron Drift Oxide Etcher with Xe Added Gas Chemistry for Low Cost and High Performance Contact Metallization**
H. Komeda, M. Hirayama, Y. Hirayama, K. Ino, R. Kaihara and T. Ohmi
Tohoku University, Japan

9:45 9B-4 **Re-distribution of Cu contamination in advanced high-speed CMOS and its influence on device characteristics**
K. Hozawa, T. Itoga, S. Isomae and M. Ohkura
Hitachi, Ltd., Japan

(Break 10:10-10:30)

Session 10A: Gate Dielectric III [Shunju I]

Chairpersons: M. Kinugawa, *Toshiba*
C. Osburn, *North Carolina State Univ.*

10:30 10A-1 A Reliable 0.1 μm Ta_2O_5 Transistor Manufactured with an Almost Standard CMOS Process
T. Devoivre, C. Papadas and M. Setton*
*ST Microelectronics and *LAM Research, France*

10:55 10A-2 Sub-Quarter Micron CMOS Process for TiN-Gate MOSFETs with TiO_2 Gate Dielectric formed by Titanium Oxidation
C. Hobbs, R. Hegde, B. Maiti, H. Tseng, D. Gilmer, P. Tobin, O. Adetutu, F. Huang, D. Weddington, R. Nagabushnam, D. O'Meara, K. Reid, L. La, L. Grove and M. Rossow
Motorola, USA

11:20 10A-3 Device and Reliability of High-K Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}
A. Chin, C.C. Liao, C.H. Lu, W.J. Chen* and C. Tsai
National Chiao Tung Univ. and National Yun-Lin Polytechnic Inst., Taiwan

11:45 10A-4 Ultra Thin high quality stack nitride/oxide gate dielectrics prepared by *in-situ* rapid thermal N_2O oxidation of NH_3-nitrided Si
S.C. Song, H.F. Luan, C.H. Lee, A.Y. Mao, S.J. Lee, J. Gelpey*, S. Marcus* and D.L. Kwong
*The University of Texas and *Steag AST Electronik, USA*

(Lunch 12:10-13:30)

Session 10B: Ferroelectric Memory Technology [Shunju II]

Chairpersons: T. Kunio, *NEC*
J. Lee, *Univ. of Texas*

10:30 10B-1 Fully functional 0.5-μm 64-kbit embedded SBT FeRAM using a new low temperature SBT deposition technique
T. Eshita, K. Nakamura, M. Mushiga, A. Itho, S. Miyagaki, H. Yamawaki, M. Aoki, S. Kishii and Y. Arimoto
Fujitsu Laboratories Limited, Japan

10:55 10B-2 A FRAM technology using 1T1C and triple metal layers for high performance and high density FRAMs
S.Y. Lee, D.J. Jung, Y.J. Song, B.J. Koo, S.O. Park, H.J. Cho, S.J. Oh, D.S. Hwang, S.I. Lee, J.K. Lee, Y.S. Park, I.S. Jung and K. Kim
Samsung Electronics Co., Korea

11:20 10B-3 Al-Interconnect/Cu-Plug Structure for FeRAM Multilevel Interconnect
S. Kishii, H. Miyazawa*, Y. Katoh*, N. Misawa*, T. Eshita and Y. Arimoto
*Fujitsu Laboratories Limited and *Fujitsu, Limited*, Japan*

11:45 10B-4 A New 1T/2C Merged Two-Terminal Gain Cell with SBT Encapsulated Floating Gate MOSFET for Highly Scalable FeRAM
M. Aoki, M. Mushiga, A. Itoh, T. Eshita and Y. Arimoto
Fujitsu Laboratories LTD., Japan

(Lunch 12:10-13:30)

Session 11A: RF Devices [Shunju I]

Chairpersons: S. Konaka, *NTT*
T.C. Chen, *IBM*

13:20 11A-1 **Transistor Design Issues in Integrating Analog Functions with High Performance Digital CMOS**
A. Chatterjee, K. Vasanth, D.T. Grider, M. Nandakumar, G. Pollack, R. Aggarwal, M. Rodder and H. Shichijo
Texas Instruments, USA

13:45 11A-2 **A 0.15-μm / 73-GHz f_{max} RF BiCMOS Technology using Cobalt Silicide Ring Extrinsic-Base Structure**
H. Suzuki, H. Yoshida, Y. Kinoshita, H. Fujii and T. Yamazaki
NEC Corporation, Japan

14:10 11A-3 **Submicron CMOS Thermal Noise Modeling from an RF Perspective**
J.J. Ou, X. Jin, C. Hu and P.R. Gray
University of California, USA

14:35 11A-4 **RF Noise Simulation for Submicron MOSFET's Based on Hydrodynamic Model**
J.-S. Goo, C.-H. Choi, E. Morifuji*, H.S. Momose*, Z. Yu, H. Iwai*, T.H. Lee and R.W. Dutton
*Stanford University, USA and *Toshiba Corporation, Japan*

(Break 15:00-15:30)

Session 11B: DRAM Technology II [Shunju II]

Chairpersons: T. Eimori, *Mitsubishi Electric*
C. Dennison, *Micron Technology*

13:20 11B-1 **New Embedded DRAM Technology using Self-aligned Salicide Block(SSB) Process for 0.18um SOC(System on a Chip)**
K. Kokubun, H. Takato, T. Sakurai, H. Koike, A. Nomachi, H. Ohtsuka, H. Harakawa, W. Sato, M. Tanaka, H. Naruse, H. Kamijo, J. Kumagai and H. Ishiuchi
Toshiba Corporation, Japan

13:45 11B-2 **Low-Temperature Metal/ON/HSG-Cylinder Capacitor Process for High Density Embedded DRAMs**
I. Yamamoto, I. Honma, T. Yamamoto, K. Urabe, K. Inoue, Y. Takaishi, Y. Yamada, K. Tokunaga, R, Kubota, M. Hamada and Y. Kato
NEC Corporation, JAPAN

14:10 11B-3 **A Novel Simple Shallow Trench Isolation (SSTI) Technology Using High Selective CeO_2 Slurry and Liner SiN as a CMP Stopper**
T. Park, J.Y. Kim, K.W. Park, H.S. Lee, H.B. Shin, Y.H. Kim, M.H. Park, H.K. Kang and M.Y. Lee
Samsung Electronics Co., Ltd., Korea (ROK)

14:35 11B-4 **Enabling Shallow Trench Isolation for 0.1 μm Technologies and Beyond**
C.-P. Chang, S.F. Shive, S.C. Kuehne, Y. Ma, H. Vuong, F.H. Baumann, M. Bude, E.J. Lloyd, C.S. Pai, M.A. Abdelgadir, R. Dail, C.T. Liu, K.P. Cheung, J.I. Colonell, W.Y.C. Lai, J.F. Miner, H. Vaidya, R.C. Liu and J.T. Clemens
Bell Laboratories, USA

(Break 15:00-15:30)

Technology for System LSI
(Technology and Circuits Joint Session) [Shunju]

Chairpersons: T.M. Liu, *TSMC*
M. Horowitz, *Stanford Univ.*

15:30 J-1 **Future perspective and scaling down roadmap for RF CMOS**
E. Morifuji, H.S. Momose, T. Ohguro, T. Yoshitomi, H. Kimijima, F. Matsuoka, M. Kinugawa, Y. Katsumata and H. Iwai
Toshiba Corporation, Japan

15:55 J-2 **Compact Distributed RLC Models for Multilevel Interconnect Networks**
J.A. Davis and J.D. Meindl
Georgia Institute of Technology, USA

16:20 J-3 **Micro IDDQ Test using Lorentz Force MOSFET's**
K. Nose and T. Sakurai
University of Tokyo, Japan

16:45 J-4 **Monte Carlo Modeling of Threshold Variation due to Dopant Fluctuations**
D.J. Frank, Y. Taur, M. Ieong and H.-S.P. Wong
IBM T.J. Watson Research Center, USA

17:30-19:30 Rump Session:

Organizers: M. Kinugawa, *Toshiba*
J. Woo, *Univ. of California*

SOI: what are the roadblocks, if any, to become a mainstream technology?
(Technology and Circuits Joint Rump Session)

Moderators: M. Yoshimi, *Toshiba*
L. DeVito, *Analog Devices*
J. Woo, *Univ. of California*

A number of companies have announced that they will employ SOI in actual LSI production. Have the issues all been settled? We would like to promote discussion among circuit designers and device/process engineers who are (or are not) interested in introducing SOI, focusing on the question ''Will SOI become a mainstream technology?''

Topics we would like to discuss include:

+ Will SOI analog/RF devices offer significant advantages over bulk Si technology?
+ Can SOI-MPUs exceed bulk Si MPUs in performance or not?
+ Can partially-depleted devices maintain advantages in very-low-power applications?
+ How can we downscale fully-depleted MOSFETs?
+ Will SOI DRAMs appear in the market?
+ How should we do with SOI design tools?
+ What is the reliability of SOI wafers?