A Bit-Line GND Sense Technique for Low-Voltage Operation FeRAM

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Abstract

We propose a sense scheme that a pMOS charge-transfer maintains bit-line level near the GND level when the plate line goes high. The scheme supplies 0.5 V higher read-out voltages across the cell capacitors and achieves a 0.4 V higher differential amplitude in a 512-cell per bit-line structure than conventional DRAM sense scheme. A Shifted bias Plate Line layout enables a minimum number of bit-lines to be activated and achieves 8.06 mW @ 3 V, 5 MHz, about same power as conventional device.