

An 84-mW 4-Gb/s Clock and Data Recovery Circuit for Serial Link Application

A 4Gb/s serial link tracking clock and data recovery (CDR) circuit fabricated in 0.24mm CMOS technology dissipates 84mW and occupies 0.3mm². The input signal is 2× over-sampled by 8 offset-cancelled receive amplifiers per cycle. The samples are processed by a phase controller to position the receive clocks at the center and the edge of the data eye using a semi-digital dual delay-locked loop (DLL) [4]. The quiet-supply p-p jitter of the receive clock is 39ps with 0.34ps/ mV supply sensitivity. It allows for plesiochronous clocking with a frequency tolerance of ±400ppm. The worst case phase resolution is < 20ps