Effects of Power-Supply Parasitic Components on Substrate Noise Generation in Large-Scale Digital Circuits

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Activity controllable noise source and arrayed substrate voltage detectors use a 0.25-μm, 2.5-V CMOS technology and enable substrate noise measurements with controlled logic density/activity distributions. Effects of power-supply parasitic components on substrate noise generation in practical large-scale CMOS digital circuits are explored. Spatially distributed parasitic impedances on power-supply/return wirings cause the noise generation locally, and moreover, screen the effect of noise attenuation by parasitic capacitances of logic elements working as charge reservoirs.