Accurate Analysis of On-Chip Inductance Effects and Implications for Optimal Repeater Insertion and Technology Scaling

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Abstract

This paper introduces an accurate analysis of on-chip inductance effects for distributed *RLC* interconnects that takes the effect of both the series resistance and the output parasitic capacitance of the driver into account. Using rigorous first principle calculations, accurate expressions for the transfer function of these lines and their time-domain response have been presented for the first time. Furthermore, an optimal repeater insertion scheme for distributed *RLC* interconnects is also presented using a novel performance optimization methodology. Additionally, the impact of line inductance on interconnect performance has been analyzed in detail with especial regards to technology scaling based on the International Technology Roadmap for Semiconductors (ITRS). Contrary to conventional wisdom, it is shown that the effect of line inductance on optimized interconnect performance will actually diminish for *scaled* global interconnects.