

# **Silicon Integrated High Performance Inductors in a 0.18 $\mu$ m CMOS Technology for MMIC**

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## **ABSTRACT**

This paper presents a complete portfolio of silicon integrated inductors in a 0.18 $\mu$ m CMOS technology. In addition to inductor design, we also present a complete optimization methodology with associated modeling and key characterization. Our inductor quality factors have been enhanced by optimizing patterned ground shield and taper coils, or use Copper metallization. Quality-factor peak can further be optimized at application-specific frequency band with our optimization algorithm. To facilitate IC design with inductors, a novel model considering eddy current loss was developed. Finally, to integrate inductors into a system-chip, inductor-to-inductor and substrate-to-inductor coupling were investigated.