A 6.25 ns Random Access 0.25 um Embedded DRAM

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A new embedded DRAM architecture with uniform low latency operation was developed for computing, signal processing, and networking applications. Two hard macro blocks, 104K x 24b and 104K x 16b, were implemented in a 0.25 micron stacked capacitor blended logic DRAM process. The combination of novel control architecture, circuit design, and physical implementation permitted a simulated worst case row access cycle time of 6.25 ns.