A Stabilization Technique for Phase-Locked Frequency Synthesizers

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Abstract

A stabilization technique is presented that relaxes the trade-off between the settling speed and the magnitude of output sidebands in phase-locked frequency synthesizers. The method introduces a zero in the open-loop transfer function through the use of a discrete-time delay cell, obviating the need for resistors in the loop filter. A 2.4-GHz CMOS frequency synthesizer employing the technique settles in approximately 60 μs with 1-MHz channel spacing while exhibiting a sideband magnitude of -58.7 dBc. Designed for Bluetooth applications and fabricated in a 0.25-μm digital CMOS technology, the synthesizer achieves a phase noise of -112 dBc/Hz at 1-MHz offset and consumes 20 mW from a 2.5-V supply.