A Fully-Integrated CMOS Frequency Synthesizer with Charge-Averaging Charge Pump and Dual-Path Loop Filter for PCS- and Cellular-CDMA Wireless Systems

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This paper presents the design of a fully-integrated CMOS frequency synthesizer for PCS- and cellular-CDMA wireless systems. The proposed charge-averaging charge pump scheme suppresses fractional spurs and the VCO combined with coarse tuning improves phase noise characteristics. The improved architecture of the dual-path loop filter makes it possible to implement a large time constant on a chip. Fabricated in 0.35-μm CMOS technology, this circuit provides 10kHz channel spacing with phase noise of −106dBc/Hz at 100kHz offset.