Automatic Calibration of Modulated Σ–Δ Frequency Synthesizers

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This paper describes a sigma–delta (Σ–Δ) synthesizer for Gaussian Frequency and Minimum Shift Keying (GFSK/GMSK) modulation. The key innovation is an in–service automatic calibration circuit which tunes the phase locked loop (PLL) to compensate for process tolerance and temperature variation. The PLL, including 1.8 GHz voltage controlled oscillator (VCO), Σ–Δ modulator, and calibration circuit has been implemented in a 0.6 micron BiCMOS integrated circuit. The test chip achieves 2.5 Mbit/second using GFSK and 5.0 Mbit/second using 4-FSK.