A New Column Redundancy Scheme for Yield Improvement of High Speed DRAMs with Multiple Bit Pre-fetch Structure

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A novel dual CSL column redundancy scheme(DCCR) that can improve effectiveness of repair and minimize overhead of die area is proposed. DCCR can repair failure bits of self-half I/O block by the unit of single bit, not by CSL. DCCR can also improve the data access speed by reducing the local I/O loading.