A system LSI memory redundancy technique using an ie-Flash (inverse-gate-electrode flash) programming circuit

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A new memory redundancy technique using ie-Flash (inverse-gate-electrode flash) memory cells was developed. Ie-Flash can be fabricated by the logic CMOS process, so no additional processes are necessary in using it in system LSIs, and it can be programmed electrically by logic tester. This new redundancy technique was successfully implemented in the cache memories of a 32-bit RISC microprocessor, and it reduced testing cost and did not significantly increase the chip area.