MOS Devices with High Quality Ultra Thin CVD ZrO_2 Gate Dielectrics and Self-Aligned TaN and TaN/Poly-Si Gate Electrodes

C. H. Lee, Y. H. Kim, H. F. Luan, S. J. Lee, T. S. Jeon, W. P. Bai, and D. L. Kwong
Microelectronics Research Center, Department of Electrical and Computer Engineering
The University of Texas, Austin, TX 78758

In this paper, we have successfully fabricated and characterized self-aligned TaN and TaN/poly-Si gated n-MOSFETs with ultra thin (EOT=11Å) CVD ZrO_2 gate dielectrics. It is show that while both gate stacks show excellent leakage current and good thermal stability after a 900°C, 30sec, N_2 anneal, the TaN/poly-Si ZrO_2 devices exhibit superior thermal stability even after 1000°C 30sec N_2 anneal. In addition, the TaN/Poly-Si devices show negligible frequency dependence of CV, charge trapping, and superior TDDB characteristics, compared to TaN devices. Well-behaved N-MOSFETs with both TaN and TaN/Poly-Si gate electrodes are demonstrated.