# A 0.115 $\mu m^2$ $8F^2$ DRAM working cell with LPRD(Low_Prasitic_Resistance Device ) and poly metal gate Technology for Gigabit DRAM

Hyunpil Noh, Woncheol Cho, Kuchul Joung, Min Huh, Jaemin Ahn, Ysung Kim, Suock Jeong, Seongjoon Lee, Dongseok Kim, Hazoong Kim, Jaebuhm Suh, Jinwon Park, Sang-don Lee, and Hee-koo Yoon

R&D Division, Hyundai Electronics Industries Co., Ltd.
San 136-1, Ami-ri, Bubal-eub, Ichon-si, Kyoungki-do, 467-701, KOREA
(e-mail : hpnoh@sr.hei.co.kr, hpnoh@hmec.co.kr )

## Abstract

$8F^2$ Stack DRAM cell 0.115 $\mu m^2$ size has been successfully integrated employing selective epitaxial plug scheme for landing plug contacts and poly metal gates and MIM COB capacitors, of which cell working has been proven under easy function check mode. Cell transistor exhibits a sufficient saturation current($I_{OP}$) of >40 $\mu A$ with threshold voltage ($V_{tsat}$) of 1.0V.