High performance 40 nm vertical MOSFET within a conventional CMOS process flow

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We present 40 nm vertical MOSFETs fabricated using the most standard CMOS process flow. At the expense of four additional but conventional steps, both planar and vertical devices can be co-integrated within the same flow. Our process is fully described and the vertical transistors are characterized. Very good device performances are reached with relaxed gate oxide thickness. Our vertical MOSFET may constitute an interesting alternative for high performance planar devices in case if aggressive scaling of oxide thickness fails.