# Performance Improvement of Metal Gate CMOS Technologies

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Metal gate CMOS technologies for high speed application was investigated using damascene metal gate process. We demonstrated the performance improvement by no gate depletion effect of metal gate using actual device. Ti/W was used as single work function metal gate material and ultra shallow buried channel profile was formed for threshold voltage control. Self-aligned channel structure effectively reduces source/drain junction capacitance. Extremely good metal/$SiO_2$ interface with CVD-TiN gate stack realizes intrinsic channel mobility. Propagation delay time of CMOS inverter ring oscillator was 20 ps, and projected performance in next generation would be better using improved technologies.