Deep Sub-Micron CMOS Device Design for Low Power Analog Applications

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This paper presents a comprehensive study on optimization of deep sub-micron NMOS device for low power analog applications. It is shown that novel channel engineering is essential along with thin gate oxides and shallow junctions for improving the device analog performance. The Single Pocket devices suppress the SCE effectively and have smaller CLM, thereby improving the analog performance. Experimental results show that, for a constraint on power supply voltage and oxide thickness, the Single Pocket devices are attractive for deep sub-micron low power analog applications.