Abstract:

A 0.13µm CMOS Platform with Cu/ Low-k Interconnects for System On Chip Applications

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We describe an advanced 0.13µm CMOS technology platform optimized for density, performance, low power and analog/mixed signal applications. Up to 8 levels of Copper interconnect with industries first true low-k dielectric (SiLK, k=2.7) result in superior interconnect performance at aggressive pitches. A 2.28µm^2 SRAM cell is manufactured with high yield by introducing elongated local interconnects on the contact level without increasing process complexity. Trench based embedded DRAM is offered for large area memory. Modular analog devices as well as passive components like resistors, MIM capacitors and intrinsic inductors are integrated.