A High Performance 0.12 mm CMOS with Manufacturable 0.18 mm Technology

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High-performance 0.12 μm CMOS devices with manufacturable 0.18 μm technology are presented. A high drive current is achieved by reducing a body effect. The double-sidewall structure can reduce the gate-fringe capacitance without increasing the junction leakage, and the inverter delay of 11 ps/stage is achieved at a nominal L_{GATE} of 0.12 μm. Small 6T-SRAM cells of 3.1 μm^2 are implemented using a vertical well isolation and a self-aligned contact. The 9-level copper interconnection is optimized.