# SOI-Optimized 64-bit High-Speed CMOS Adder Design

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We present a high-speed 64-bit hybrid carry-lookahead/ carry-select adder in 0.1μm partially depleted silicon-on-insulator (PD/SOI) technology with a critical path delay of 346ps. Sense–amplifier based differential logic with source follower evaluation tree is used for fast generation of 8-bit group carry. Floating body PD/SOI shows 24% performance improvement over bulk CMOS for the 8-bit group carry generating circuit. We also show that the proposed circuit is robust to noise induced by floating body effect in PD/SOI.