SESO Memory: A CMOS compatible high density embedded memory technology for mobile applications

Bryan Atwood, Tomoyuki Ishii, Taro Osabe, Toshiyuji Mine, Fumio Murai, Kazuo Yano
Central Research Laboratory, Hitachi, Ltd. Kokubunji Tokyo 185-8601, Japan

SESO memory is proposed as a dense, low power embedded memory. Incorporating an ultra-low leakage thin-film transistor (SESO), this memory has a cell area almost three times smaller than conventional SRAM and requires no additional processing materials. Fabricated SESO characteristics are presented and a 3-transistor cell structure is designed to accommodate an array access time of 10 ns, showing SESO memory to be a strong candidate as an inexpensive embedded memory.