An Accurate and Efficient Analysis Method for Multi-Gb/s Chip-to-chip Signaling Schemes

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This paper introduces an accurate method of modeling the performance of high-speed chip-to-chip signaling systems. Implemented in a simulation tool, it precisely accounts for intersymbol interference, cross-talk and echos as well as circuit related effects such as thermal noise, power supply noise and receiver jitter. We correlated the simulation tool to actual measurements of a high-speed signaling system and then used this tool to make tradeoffs between different methods of chip-to-chip signaling with and without equalization.