Novel Polycrystalline Gate Engineering for High Performance Sub-100 nm CMOS Devices

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Abstract

We have developed a design for a polycrystalline (poly-) gate in high performance sub-100 nm CMOS devices. The inversion capacitance was found to obviously decrease as the gate length becomes shorter below 100 nm. This phenomenon is explained as follows: (1) the gate length becoming shorter than the poly-grain size (R_G) and (2) the short dopant-diffusion length from grain boundaries (D_H). Techniques for achieving small R_G and large D_H improved the I_D figures by +15% and +3% for the p- and n-FET that have 65-nm poly-SiGe gates.