A 45 nm Gate Length High Performance SOI Transistor for 100nm CMOS Technology Applications

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Abstract

Partially depleted SOI transistors with gate lengths down to 45nm reach self-heated drive currents of 940uA/um and 460uA/um at 20nA/um for NMOS and PMOS, respectively. A measured median stage delay of 6 picoseconds was achieved on an inverter-fan-out-1 ring oscillator at 1.3V at a total N+P leakage of 30nA/um. The exceptional AC performance of this technology is among the highest reported in the literature at this low transistor leakage and operating voltage.