Sub-1μm^2 High Density Embedded SRAM Technologies for 100nm Generation SOC and Beyond

K. Tomita, K. Hashimoto, T. Inbe, T. Oashi, K.Tsukamoto, Y. Nishioka, M. Matsuura, T. Eimori and M. Inuishi
ULSI Development Center, Mitsubishi Electric Corp.
Hyogo 664-8641, Japan
I. Miyanaga, M. Nakamura, T. Kishimoto, T. Yamada, K. Eriguchi, H. Yuasa, T. Satake, A. Kajiya and M. Ogura
ULSI Process Technology Development Center, Semiconductor Company, Matsushita Electric Industrial Co., Ltd.
Kyoto, 601-8413, Japan

We have integrated high speed and high density 6T-SRAM cell of 0.998μm^2 for system-on-a-chip (SOC) using enhanced 100nm CMOS logic technology. This is achieved by the systematic integration methodology, which includes high-NA ArF lithography, optimized optical proximity correction (OPC) CAD, narrow well isolation, poly-buffered shallow trench isolation (STI), offset spacer transistor, 9-level Cu interconnect and low-k dielectric technologies with the lithographically scalable SRAM cell design.