Low Standby Power CMOS with HfO_2 Gate Oxide for 100-nm Generation

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We have fabricated 55-nm poly-Si gated n- and p-MOSFETs with HfO_2 gate dielectric of 3-nm physical thickness deposited by atomic layer deposition (ALD). Conventional CMOS process was used with high-temperature sorce-drain anneal of $\geq 1000^0$ C, cobalt-silicide and pocket implant. The devices showed very promising characteristics for low standby power applications due to drastic reduction of gate leakage current.