Impact of Joule Heating on Scaling of Deep Sub-Micron Cu/low-k Interconnects

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Abstract

This paper investigates the impact of Joule heating on the scaling trends of advanced VLSI interconnects. It shows that the interconnect Joule heating can strongly affect the maximum operating temperature of the global wires which, in turn, will constrain the scaling of current density to mitigate electromigration and, thus greatly degrade the expected speed improvement from the use of low-k dielectrics. Through a combination of extensive electrothermal simulation and 2D field solver for capacitance calculation, the thermal characteristics of various Cu/low-k schemes are quantified and their effects on electromigration reliability and interconnect delay is determined. The effect of vias, as efficient heat conduction paths, is included for realistic evaluation.