A 64Mbit Embedded FeRAM Utilizing a 130nm, 5LM Cu/FSG Logic Process

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A low-voltage (1.3V), 64Mbit Ferroelectric Random Access Memory using a 1-transistor, 1-capacitor (1T1C) cell is demonstrated. This is the largest FRAM memory demonstrated to date. The memory is constructed using a state-of-the-art 130nm transistor and a five-level Cu/FSG interconnect process. Only two additional masks are required for integration of the ferroelectric module into a single-gate oxide, low-voltage logic process. Address access time for the memory is less than 30ns while consuming 0.57mW/MHz at 1.37V. An eFRAM density of 1.13 Mb/mm^2 is achieved with a cell size of 0.54um^2 and capacitor size of 0.25um^2.