Abstract

"A Design of a Compact 2GHz-PLL with a New Adaptive Active Loop Filter Circuit"

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A compact active loop filter for PLL with adaptive biasing technique is described. Using the new filter, the PLL can automatically adjust the loop bandwidth and the damping factor to the frequency of the reference clock. Moreover, the filter can decrease the capacitance value to 1/10-1/20 of conventional one. A test chip was fabricated in 0.15μm-CMOS process. The PLL can reduce the chip area to 1/2 of the conventional one while keeping good jitter performance.