A Low jitter, Fast recoverable, Fully analog DLL using Tracking ADC For High Speed and Low Stand-by power DDR I/O interface

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Abstract

For high bandwidth and low stand-by power DDR (Double Data Rate) I/O interface, a new fully analog DLL (Delay Locked Loop) are designed and implemented in 0.16μm DRAM process. Utilizing a tracking ADC (Analog-to-Digital Converter), a large stand-by current of the analog DLL is suppressed without losing locking information nor compromising jitter performance. Two-step duty correction scheme using multiphase clocks and phase mixing corrects an inherent duty-error of a system clock with more precision and speed, especially for a large duty-error. Proposed DLL has a 100MHz~ 520MHz wide lock-range and a 65psec peak-to-peak jitter and 0.064psec/mv supply sensitivity at 2.3v supply voltage consuming 1.1mA of stand-by current.