

Clock Generation and Distribution for the Third Generation Itanium® Processor

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Abstract

The clock generation and distribution system for the third generation Itanium® processor operates at 1.5GHz with a skew of 24ps. Significant enhancements have been added to the current design to enable post-silicon clock optimization for higher performance. Electrically programmable fuses enable the post-silicon speed path balancing for higher performance. 69 fuses support 23 clock buffer zones. The scan chain complements fuses and an optimization algorithm has been established to search for the best fuse settings.