A 0.9V 9mW 1MSPS Digitally Calibrated ADC with 75dB SFDR

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Abstract

A low-voltage two-stage algorithmic ADC incorporating the Opamp-Reset Switching Technique (ORST) is presented. The low-voltage digital CMOS process compatible operation is achieved without the clock boosting/bootstrapping or switched-opamp. The ADC employs a highly linear input sampling circuit at the front-end, and the digital output is calibrated using a radix-based scheme. The prototype was fabricated in a 0.18μm CMOS technology and the active die area is 1.2mm x 1.2mm. The calibrated ADC demonstrates 75dB SFDR at 0.9V and 80dB SFDR at 1.2V. The total power consumption of the ADC is 9mW at the clock frequency of 7MHz (1MSPS).