A 27-mW 3.6-Gb/s I/O Transceiver

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Abstract

This paper describes a 3.6-Gbps 27-mW transceiver for chip-to-chip applications. A novel data receiving and timing recovery technique are presented with very low power penalties while maintaining high signal integrity. The input comparator filters noise with built-in bandwidth control and digital offset compensation while consuming 300uW. Static phase offset introduced onto the charge-pump permits phase recovery with no additional power. The entire design occupies $0.2mm^2$ in a 0.18-um 1.8-V CMOS technology.