

# **Strained FIP-SOI (FinFET/FD/PD-SOI) for Sub-65 nm CMOS Scaling**

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A highly manufacturable SOI technology with strained silicon and FinFET-like devices is demonstrated for sub-65 nm device scaling. This technology, named FIP-SOI (FinFET/FD/PD-SOI), achieves (1) performance gain of 10-35% for N-MOS using strained silicon compared with non-strained SOI, (2) bulk-to-SOI design portability without additional structures such as the body-contacted transistor scheme, and (3) superior scalability by the incorporation of FinFET-like devices. All feature size scaling will further enhance channel strain in the FIP-SOI. Scaling-strengthened strain is demonstrated for the first time.